LEOPARD IMAGING INC

Rev. 1.0

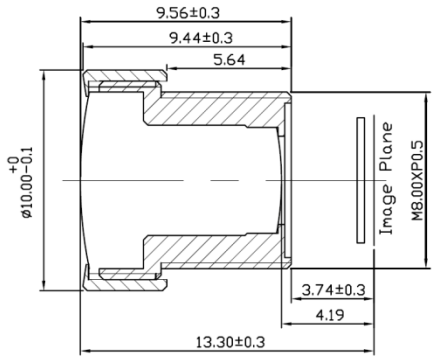
LI-V024M-MIPI-IPEX30 Data Sheet

Key Features

- Aptina 1/3" Wide-VGA CMOS Digital Image Sensor MT9V024
- Optical format: 1/3"
- Active pixels: 752H x 480V
- Pixel size: 6.0 um x 6.0 um
- Global shutter
- True RAW Data Output
- Color filter array: Monochrome
- Support 752 x 480 @ 60 fps
- Build-in Parallel to MIPI Bridge
- Support M8 lens
- Mating I-PEX cable: FAW-1233
- Support multiple cable length options
- Module Size: 27mm x 19mm
- Weight: 3 g
- Part#: LI-V024M-MIPI-IPEX30

Lens Spec

- Part#: HK-8055-J1-M8
- Sensor size: 1/3"
- Focal Length: 2.35 mm
- Aperture, F/#: 2.5
- Built in 650 nm IR cut filter
- FOV (D/H/V): 115°/90°/65°
- Mount: M8 x P0.5 – 6g



Application

- Automotive
- Smart vision
- Video as input
- Machine vision

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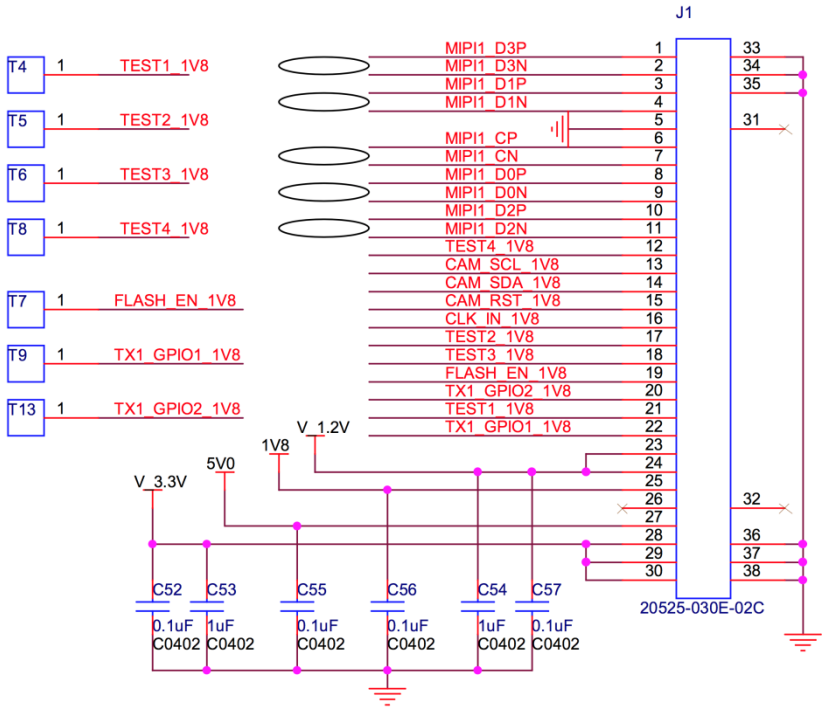
Pin Assignment

Interface J1:

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.5	V
I_{SUPPLY}	Total power supply current	-	200	mA
I_{GND}	Total ground current	-	200	mA
V_{IN}	DC input voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	DC output voltage	-0.3	V_{DD} + 0.3	V
T_{STG}^{Note}	Storage temperature	-50	+150	°C

Note: This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC Electrical Characteristics Over Temperature

VPWR = 3.3V ±0.3V; TJ = – 40°C to +105°C; Output Load = 10pF; Frequency 13 MHz to 27 MHz; LVDS off

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH voltage		V_{PWR} - 1.4	-		V
V_{IL}	Input LOW voltage			-	1.3	V
I_{IN}	Input leakage current	No pull-up resistor; $V_{IN} = V_{PWR}$ or V_{GND}	-5	-	5	µ A
V_{OH}	Output HIGH voltage	I_{OH} = –4.0mA	V_{PWR} - 0.3	-	-	V
V_{OL}	Output LOW voltage	I_{OL} = 4.0mA	-	-	0.3	V
I_{OH}	Output HIGH current	$V_{OH}=V_{DD}$-0.7	-11	-	-	mA
I_{OL}	Output LOW current	V_{OL} = 0.7	-	-	11	mA
$I_{PWR}A$	Analog supply current	Default settings	-	12	20	mA
I_{PIX}	Pixel supply current	Default settings	-	1.1	3	mA
$I_{PWR}D$	Digital supply current	Default settings, C_{LOAD} = 10pF	-	42	60	mA
I_{LVDS}	LVDS supply current	Default settings with LVDS on	-	13	16	mA
$I_{PWR}A$ Standby	Analog standby supply current	STDBY = V_{DD}	-	0.2	3	µ A
$I_{PWR}D$ Standby Clock Off	Digital standby supply current with clock off	STDBY = V_{DD}, CLKIN = 0 MHz	-	0.1	10	µ A
$I_{PWR}D$ Standby Clock On	Digital standby supply current with clock on	STDBY= V_{DD}, CLKIN = 27 MHz	-	1	2	mA

DC Electrical Characteristics

VPWR = 3.3V ±0.3V; TA = Ambient = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
LVDS Driver DC Specifications						
$\|V_{OD}\|$	Output differential voltage	R_{LOAD} = 100 Ω ± 1%	250	-	400	mV
$\|DV_{OD}\|$	Change in V_{OD} between complementary output states		-	-	50	mV
V_{OS}	Output offset voltage		1.0	1.2	1.4	mV
DV_{OS}	Pixel array current		-	-	35	mV
I_{OS}	Digital supply current			±10		mA
I_{OZ}	Output current when driver is tri- state			±1		µ A
LVDS Receiver DC Specifications						
V_{IDTH+}	Input differential	$\|V_{GPD}\| < 925mV$	-100	-	100	mV
Iin	Input current		-	-	±20	µ A

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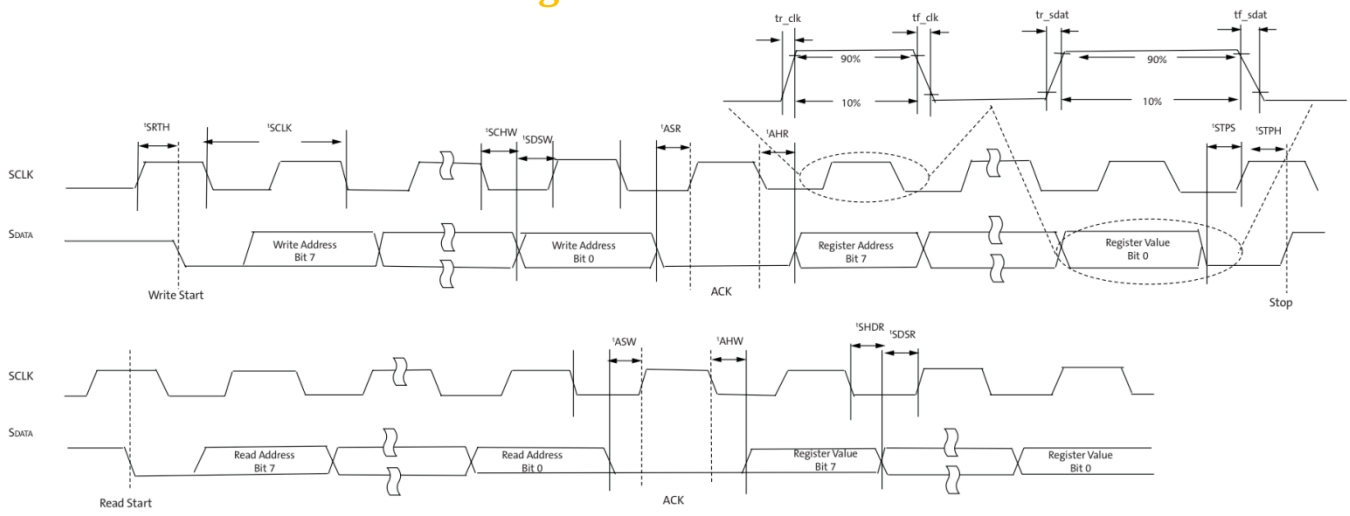
Two-Wire Serial Bus Timing



Test Conditions: 25°C, 26.67 MHz, and 3.3V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock frequency				400	kHz
^{t}SCLK	Serial Input clock period				2.5	µ sec
	SCLK duty cycle	When active	40	50	60	%
^{t}r_sclk	SCLK rise time			165		ns
^{t}f_sclk	SCLK fall time			6		ns
^{t}r_sdat	S_{DATA} rise time	1.5 kΩ pull-up		180		ns
^{t}f_sdat	S_{DATA} fall time			9		ns
^{t}SRTS	Start setup time	WRITE/READ	148	150	167	ns
^{t}SRTH	Start hold time	WRITE/READ	36.9	36	37.6	ns
^{t}SDSW	S_{DATA} setup	WRITE	0	5	12	ns
^{t}SDHW	S_{DATA} hold	WRITE	1.3	36	37	ns
^{t}ASW	ACK setup time	WRITE	146	146	148	ns
^{t}AHW	ACK hold time	WRITE	98.9	107	144	ns
^{t}STPS	Stop setup time	WRITE/READ		624		ns
^{t}STPH	Stop hold time	WRITE/READ		1.61		ns
^{t}ASR	ACK setup time	READ	192	228	229	ns
^{t}AHR	ACK hold time	READ	247	284	287	ns
^{t}SDSR	S_{DATA} setup	READ	654	655	690	ns
^{t}SDHR	S_{DATA} hold	READ	560	595	596	ns
CIN_SI	Serial interface input pin capacitance			3.5		ns
CLOAD_SD	S_{DATA} max load capacitance			15		ns
RSD	S_{DATA} external pull-up resistor			1.5		kΩ

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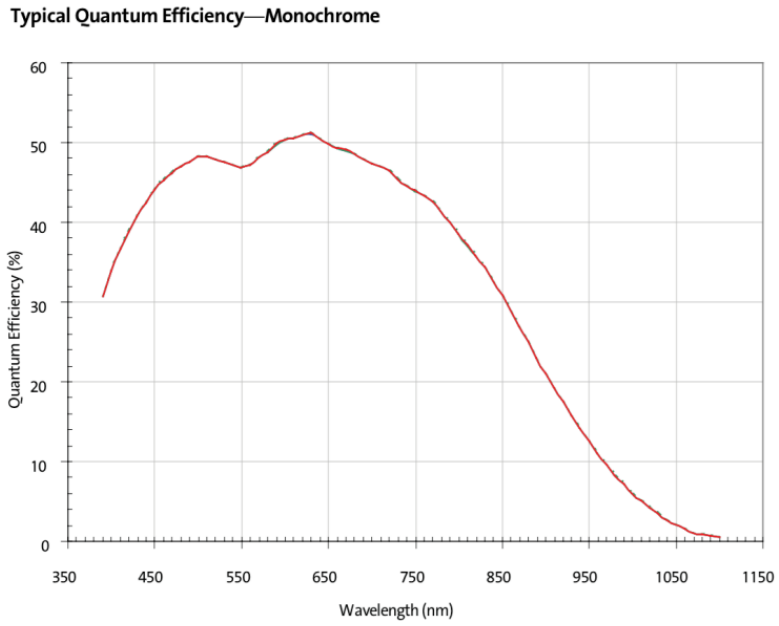
AC Electrical Characteristics

VPWR = 3.3V ±0.3V; TJ = –40°C to +105°C; Output Load = 10pF

Symbol	Definition	Condition	Min	Typ	Max	Unit
SYSCLK	Input clock frequency		13.0	26.6	27.0	MHz
	Clock duty cycle		45.0	50.0	55.0	%
^{t}R	Input clock rise time		-	3	5	ns
^{t}F	Input clock fall time		-	3	5	ns
$^{t}PLH_{P}$	SYSCLK to PIXCLK propagation delay	C_{LOAD} = 10pF	4	6	8	ns
^{t}PD	PIXCLK to valid $D_{OUT}(9:0)$ propagation delay	C_{LOAD} = 10pF	-3	0.6	3	ns
^{t}SD	Data setup time		14	16	-	ns
^{t}HD	Data hold time		14	16		
$^{t}PFLR$	PIXCLK to LV propagation delay	C_{LOAD} = 10pF	5	7	9	ns
$^{t}PFLF$	PIXCLK to FV propagation delay	C_{LOAD} = 10pF	5	7	9	ns

Spectral characteristics



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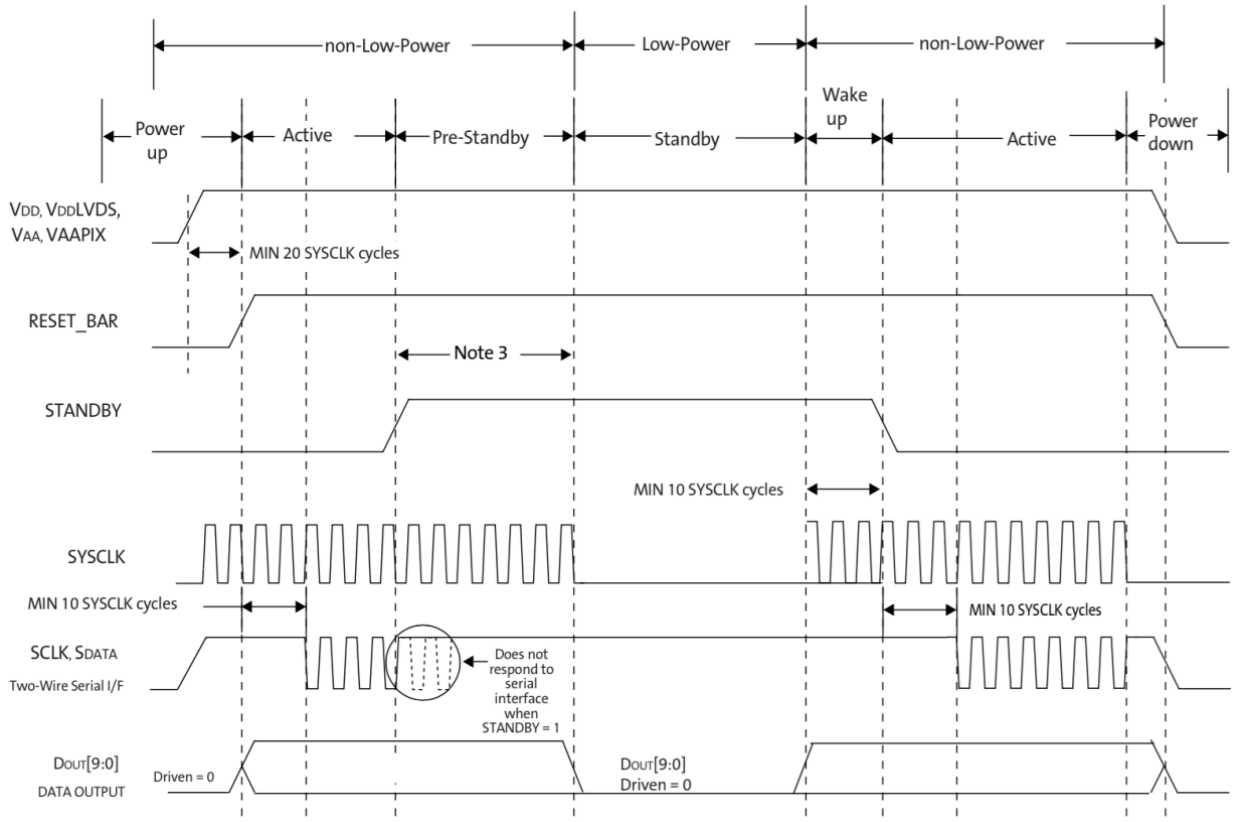
Power-up, Reset, Clock, and Standby Sequence



Note: 1. All output signals are defined during initial power-up with RESET_BAR held LOW without SYSCLK being active. To properly reset the rest of the sensor, during initial power-up, assert RESET_BAR (set to LOW state) for at least 750ns after all power supplies have stabilized and SYSCLK is active (being clocked). Driving RESET_BAR to LOW state does not put the part in a low power state

2. Before using two-wire serial interface, wait for10 SYSCLK rising edges after RESET_BAR is de-asserted.
3. Once the sensor detects that STANDBY has been asserted, it completes the current frame readout before entering standby mode. The user must supply enough SYSCLKs to allow a complete frame readout.
4. In standby, all video data and synchronization output signals are driven to a low state.
5. In standby, the two-wire serial interface is not active.

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