

LI-AR0144-MIPI-85H SPECIFICATION

**Rev 1.0
Leopard Imaging Inc.**

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Version History

Version	Description	Release Date
1.0	First Release	13. Jul. 2017



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Key Information

Module Part#		LI-AR0144-MIPI-85H
Module Size		37 mm (L) x 8 mm (W) x 5.6 mm(H)
Sensor Type		AR0144
Array Size		1280 x 800
Supply Voltage	Digital	1.2V
	Analog	2.8V
	I/O	1.8 or 2.8V
Optical format		1/4" (4.5mm)
Focus(F.NO)		2.2
FOV (H)		85°
Focal Length		2.3 mm
Focusing Range		20cm to Infinity
TV Distortion		< -20 %
Pixel size		3.0 um x 3.0 um
Color filter array		Monochrome
Output format		Raw data
Operating temperature		-40°C to +85°C (ambient) -40°C to +105°C (junction)
Max. Frame Rate		Full resolution @ 60fps 720P @ 66fps
Dynamic Range		63.9 dB
SNR _{MAX}		38 dB
Responsivity		3.6 V/lux-sec (Monochrome)
Shutter type		Global shutter
Power consumption		< 250mW
Input clock range		6 ~ 64MHz
Output pixel clock maximum		74.25 MHz



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Pin Assignment

No.	Name	Pin type	Description
1	SDA	I/O	Two-Wire Serial data I/O
2	SCL	Input	Two-Wire Serial clock input
3	DOVDD 1.8V	Power	I/O supply power
4	MCP	Output	MIPI serial clock differential P
5	MCN	Output	MIPI serial clock differential N
6	DGND	Power	Digital GND
7	MDP1	Output	MIPI serial data, lane 1, differential P
8	MDN1	Output	MIPI serial data, lane 1, differential N
9	DGND	Power	Digital GND
10	MDP2	Output	MIPI serial data, lane 2, differential P
11	MDN2	Output	MIPI serial data, lane 2, differential N
12	DGND	Power	Digital GND
13	NC	NC	
14	SHUTTER	Output	Control signal to drive external light sources
15	AGND	Power	Analog GND
16	TRIGGER	Input	Exposure synchronization input
17	SADDR	Input	Two-Wire Serial address select
18	DVDD 1.2V	Power	Digital power
19	XCLK	Input	External input clock
20	FLASH	Output	Control signal to drive external light sources
21	RESET	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
22	AVDD 2.8V	Power	Analog power
23	NC	NC	
24	DGND	Power	Digital GND



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Electrical Characteristics

1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
VSUPPLY	Power supply voltage (all supplies)	-0.3	4.5	V	VSUPPLY
ISUPPLY	Total power supply current	-	200	mA	ISUPPLY
IGND	Total ground current	-	200	mA	IGND
VIN	DC input voltage	-0.3	VDD_IO + 0.3	V	VIN
VOUT	DC output voltage	-0.3	VDD_IO + 0.3	V	VOUT
TSTG ¹	Storage temperature	-40	+125	°C	TSTG ¹

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Operating Current Consumption for MIPI Output

VAA = VAA_PIX = VDD_IO = 2.8V; VDD = VDD_PHY = 1.2V; PLL Enabled and PIXCLK = 74.25 MHz; TA = 55°C;
CLOAD = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	MIPI, Streaming, Full resolution 60 fps	IDD				mA
I/O digital operating current	MIPI, Streaming, Full resolution 60 fps	IDD_IO				mA
Analog operating current	MIPI, Streaming, Full resolution 60 fps	IAA				mA
Pixel supply current	MIPI, Streaming, Full resolution 60 fps	IAA_PIX				mA
PLL supply current	MIPI, Streaming, Full resolution 60 fps	IDD_PLL				mA
PHY supply current	MIPI, Streaming, Full resolution 60fps	IDD_PHY				mA

3. DC Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD	Core digital voltage		1.14	1.2	1.26	V
VDD_IO	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
VAA	Analog voltage		2.5	2.8	3.1	V
VAA_PIX	Pixel supply voltage		2.5	2.8	3.1	V
VDD_PHY	MIPI supply voltage		1.14	1.2	1.26	V
VIH	Input HIGH voltage		VDD_IO * 0.7	-	-	V
VIL	Input LOW voltage		-	-	VDD_IO * 0.3	V
IIN	Input leakage current	No pull-up resistor; VIN = VDD_IO or DGND	20	-	-	μA
VOH	Output HIGH voltage		VDD_IO - 0.3	-	-	V
VOL	Output LOW voltage	VDD_IO = 2.8V	-	-	0.4	V
IOH	Output HIGH current	At specified VOH	-22	-	-	mA
IOL	Output LOW current	At specified VOL	-	-	22	mA

Caution Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.



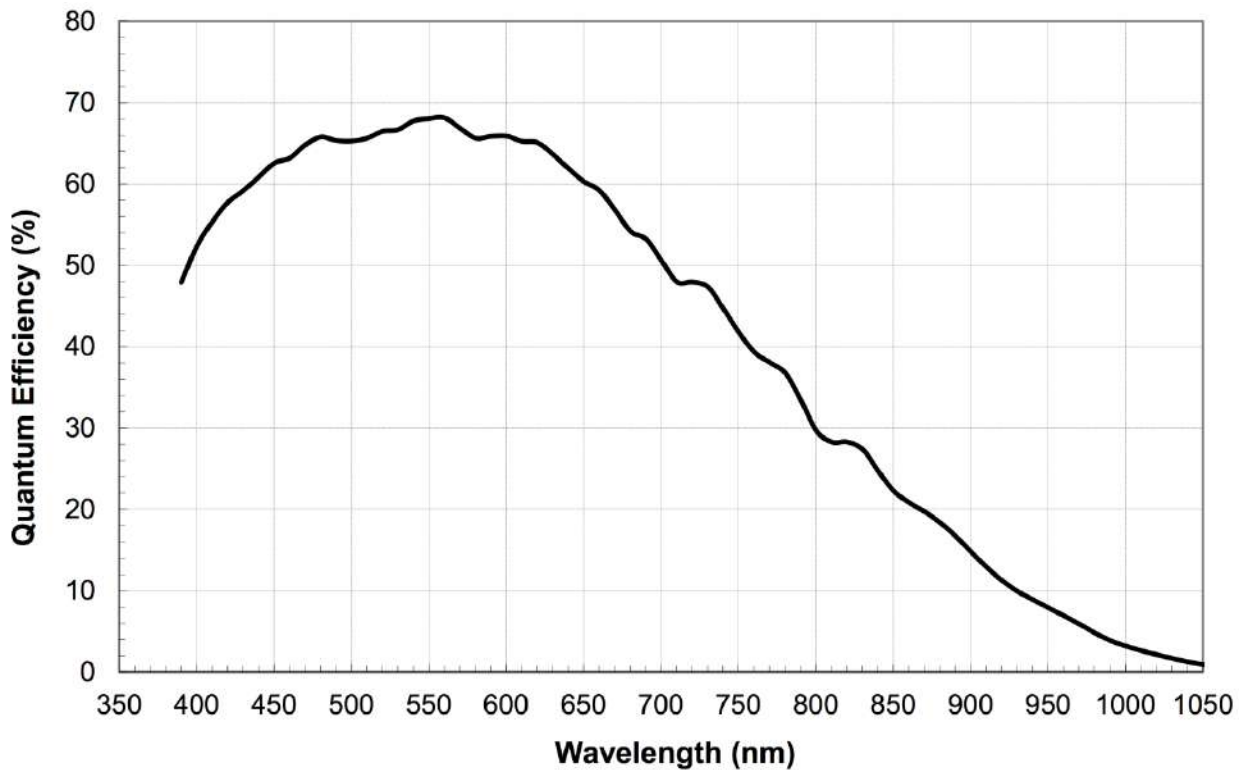
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4. Standby Current Consumption

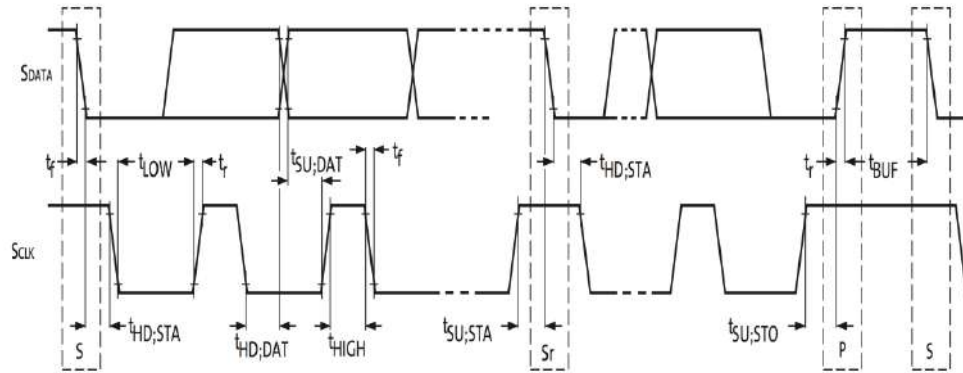
Analog - VAA + VAA_PIX; Digital - VDD + VDD_PHY; T_A = 55°C

Definition	Condition	Min	Typ	Max	Unit
Soft standby (clock off, driven low)	Analog, 2.8V				μA
	Digital, 1.2V				μA
	VDD_IO, 2.8V				mA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				μA
	Digital, 1.2V				mA
	VDD_IO, 2.8V				mA
Hard reset (clock off, driven low)	Analog, 2.8V				μA
	Digital, 1.2V				μA
	VDD_IO, 2.8V				mA
Hard reset (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				μA
	Digital, 1.2V				μA
	Analog, 2.8V				mA

5. Quantum Efficiency - Monochrome Sensor (Typical)



6. Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

7. Two-Wire Serial Bus Characteristics

$f_{EXTCLK} = 27 \text{ MHz}$; $V_{DD} = 1.2\text{V}$; $V_{DD_IO} = 2.8\text{V}$; $V_{AA} = 2.8\text{V}$; $V_{AA_PIX} = 2.8\text{V}$; $V_{DD_PHY} = 1.2\text{V}$; $T_A = 25^\circ\text{C}$

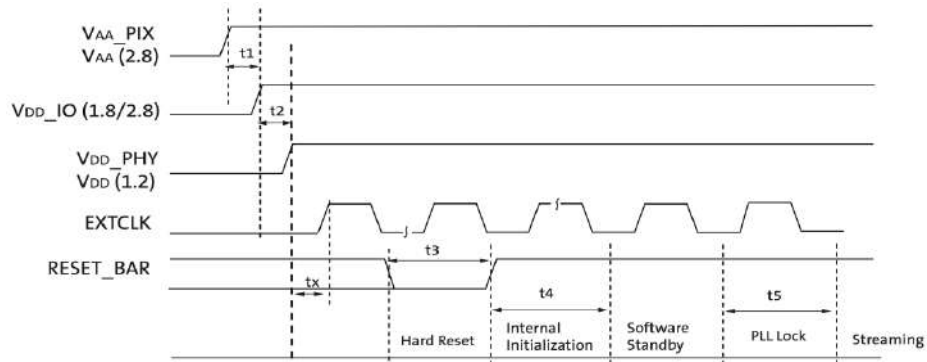
Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD,STA}$	4.0	-	0.6	-	μS
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	μS
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	μS
Set-up time for a repeated START condition	$t_{SU,STA}$	4.7	-	0.6	-	μS
Data hold time:	$t_{HD,DAT}$	0 ⁴	3.45 ⁵	0 ⁶	0.9 ⁵	μS
Data set-up time	$t_{SU,DAT}$	250	-	100 ⁶	-	nS
Rise time of both SDATA and SCLK signals	t_r	-	1000	$20 + 0.1Cb^7$	300	nS
Fall time of both SDATA and SCLK signals	t_f	-	300	$20 + 0.1Cb^7$	300	nS
Set-up time for STOP condition	$t_{SU,STO}$	4.0	-	0.6	-	μS
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μS
Capacitive load for each bus line	C_b	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	K Ω

- Notes:
1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
 2. Two-wire control is I²C-compatible.
 3. All values referred to $V_{IHmin} = 0.9 V_{DD}$ and $V_{ILmax} = 0.1V_{DD}$ levels. Sensor EXCLK = 27 MHz.
 4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
 5. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
 6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU,DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line $t_r \text{ max} + t_{SU,DAT} = 1000 + 250 = 1250 \text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCLK line is released.
 7. C_b = total capacitance of one bus line in pF.



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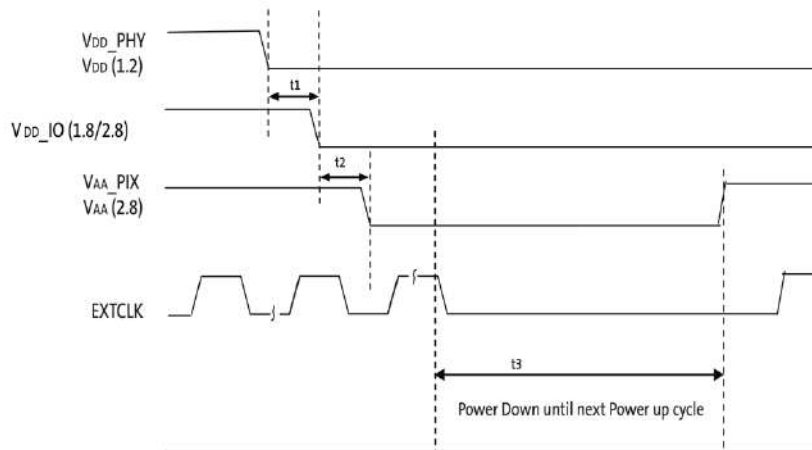
8. Power-Up Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
VAA/VAA_PIX to VDD_IO	t ₁	0	10	–	μs
VDD_IO to VDD/VDD_PHY	t ₂	0	10	–	μs
Xtal settle time	t _x	–	30 ¹	–	ms
Hard Reset	t ₃	1 ²	–	–	ms
Internal Initialization	t ₄	160000	–	–	EXTCLKs
PLL Lock Time	t ₅	1	–	–	ms

- Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
 2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

9. Power-Down Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PHY / VDD to VDD_IO	t ₁	0	–	–	μs
VDD_IO to VAA/VAA_PIX	t ₂	0	–	–	μs
PwrDn until Next PwrUp Time	t ₃	100	–	–	ms

- Note: t₃ is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.



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