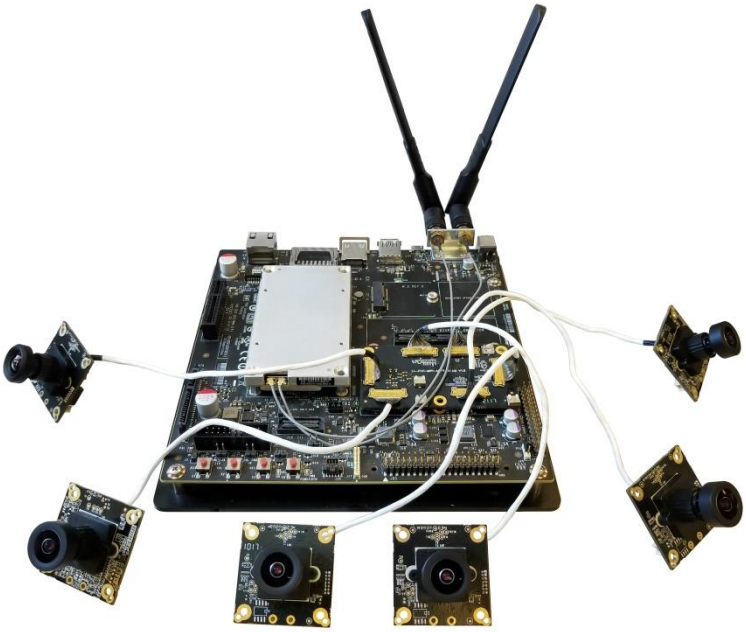
LEOPARD IMAGING INC
Rev 1.0

LI-JETSON-KIT-AR0144M12-X Data Sheet



Key Features

- Compatible with Nvidia Jetson TX1/TX2 Developer Kit
- MIPI CSI-2 interface
- Support up to six cameras
- Two adapter board options
  - LI-JTX1-MIPI-ADPT
    Includes three 4-lane interface
  - LI-JTX1-MIPI-ADPT-6CAM
    Includes six 2-lane interface
- ON Semiconductor CMOS Image Sensor AR0144
- Active pixels: 1280H x 800V
- Pixel size: 3.0 um x 3.0 um
- Global Shutter
- Monochrome sensor
- Length of the I-PEX cable: 300mm
- Support multiple length cables
- Connector Part#: 20525-030E-02C
- Support M12 x P0.5 lens
- Provide customization services
- Part#:

(1 cam) LI-JETSON-KIT-AR0144M12
(2 cam) LI-JETSON-KIT-AR0144M12-D
(3 cam) LI-JETSON-KIT-AR0144M12-T
(6 cam) LI-JETSON-KIT-AR0144M12-H

Lens Spec

- Model: SYD1201A
- Focal length: 3.7 mm
- Aperture, F/#: 2.8 +/- 5%
- Built in 650nm IR cut filter
- FOV (D/H/V): 66.5 °/ 59 °/35.5 °
- TV Distortion: -1.0 %

BOM

Nvidia TX1/TX2 Developer Kit not included

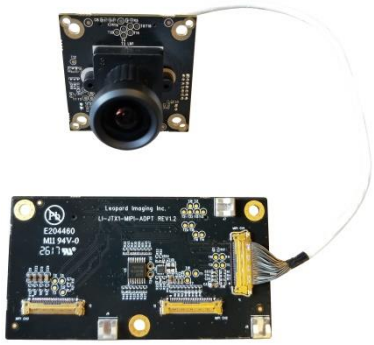
#	Items	QTY
1	LI-JTX1-MIPI-ADPT or LI-JTX1-MIPI-ADPT-6CAM	1
2	LI-AR0144-MIPI-M12	1,2,3 or 6
3	FAW-1233-03 cable	1,2,3 or 6

Leopard Imaging Inc.
48820 Kato Rd, Suite 100B, Fremont, CA 94538, USA
Phone: +1-408-263-0988
Fax: +1-408-217-1960
Email:sales@leopardimaging.com
Website: www.leopardimaging.com

LI-JETSON-KIT-AR0144M12

BOM

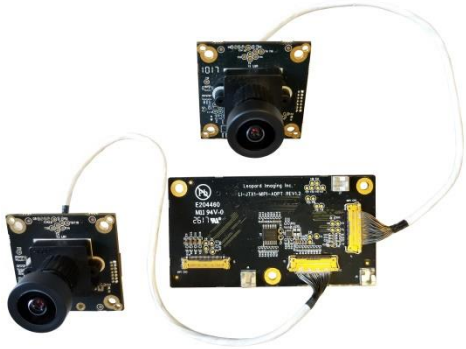
#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-AR0144-MIPI-M12	1
3	FAW-1233-03 cable	1



LI-JETSON-KIT-AR0144M12-D

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-AR0144-MIPI-M12	2
3	FAW-1233-03 cable	2



LI-JETSON-KIT-AR0144M12-T

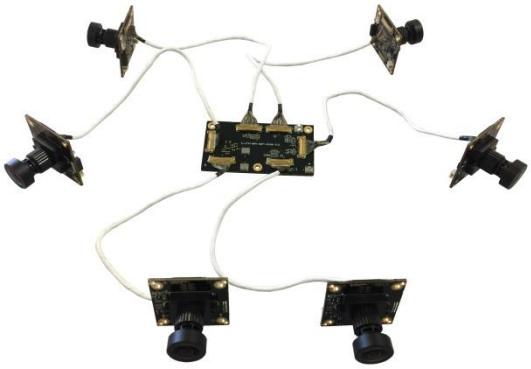
BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-AR0144-MIPI-M12	3
3	FAW-1233-03 cable	3

LI-JETSON-KIT-AR0144M12-H

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT-6CAM	1
2	LI-AR0144-MIPI-M12	6
3	FAW-1233-03 cable	6



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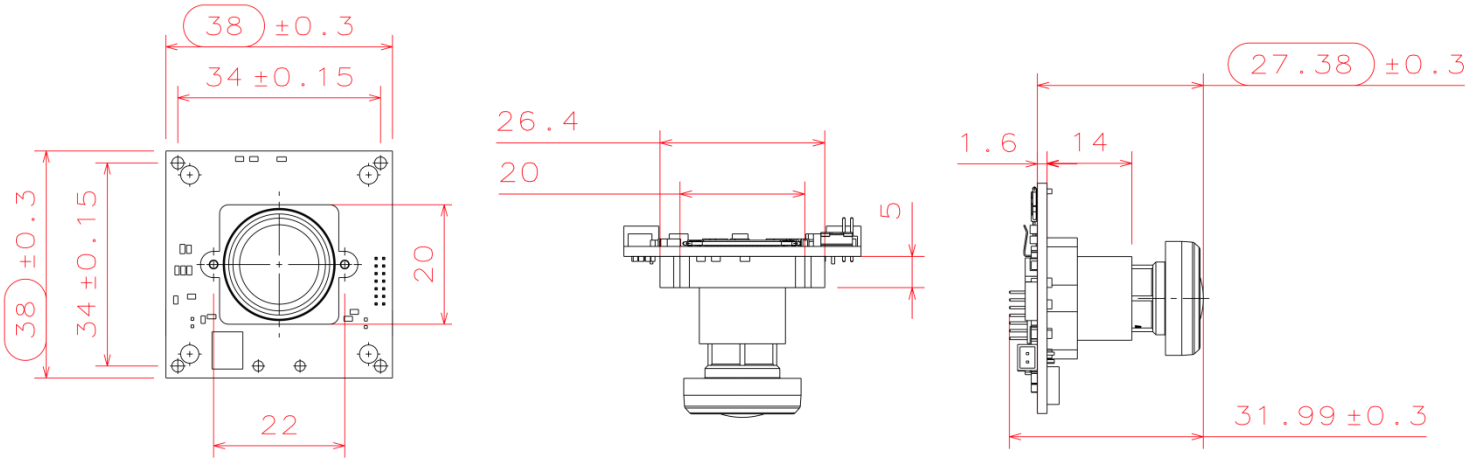
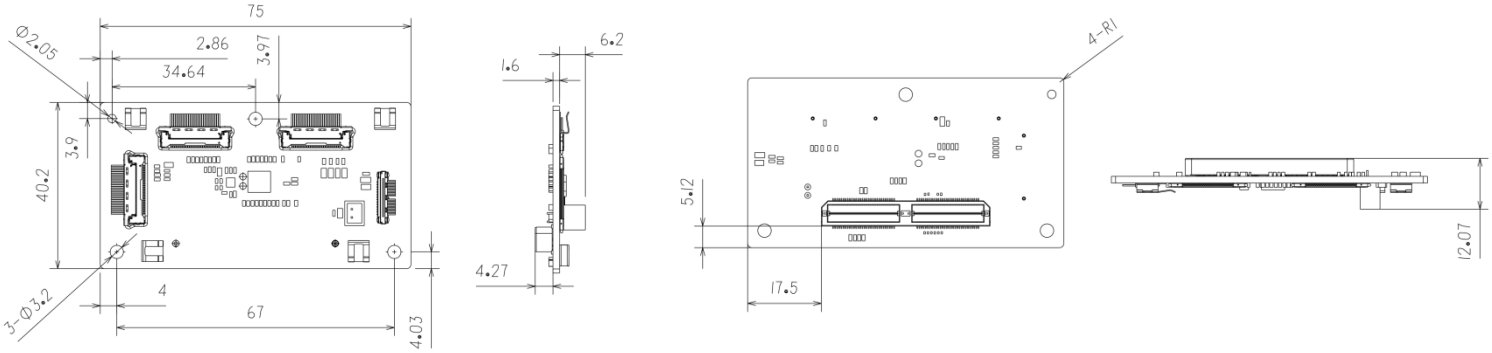
Dimensions

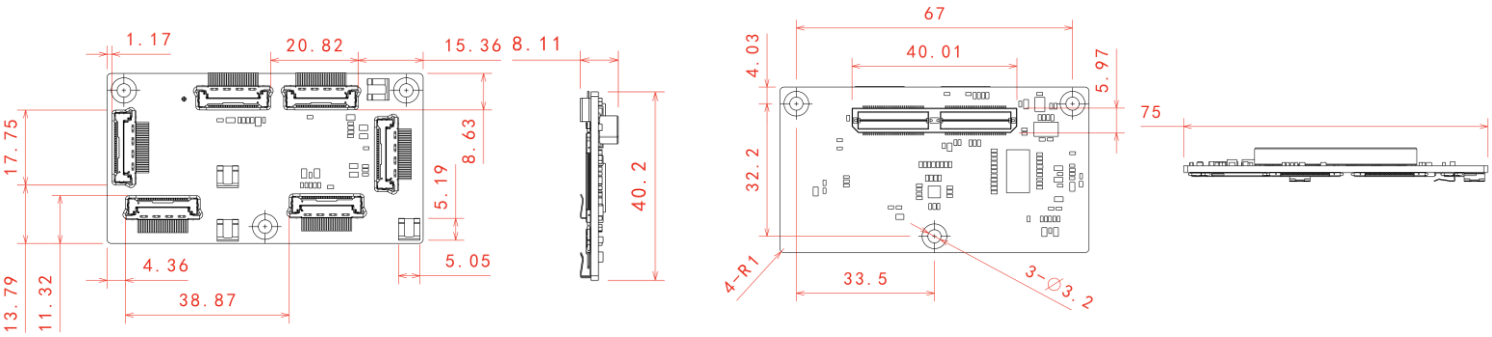
LI-AR0144-MIPI-M12



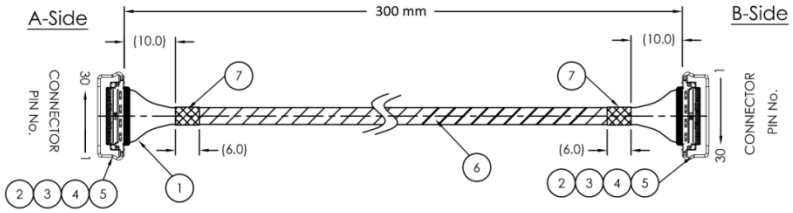
LI-JTX1-MIPI-ADPT



LI-JTX1-MIPI-ADPT-6CAM



FAW-1233-03



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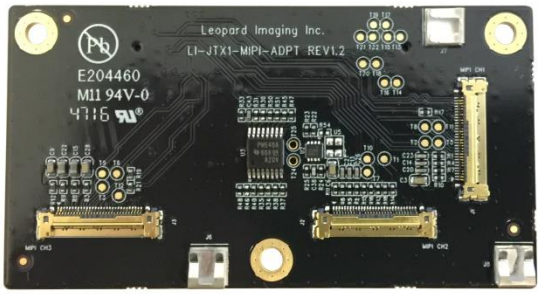
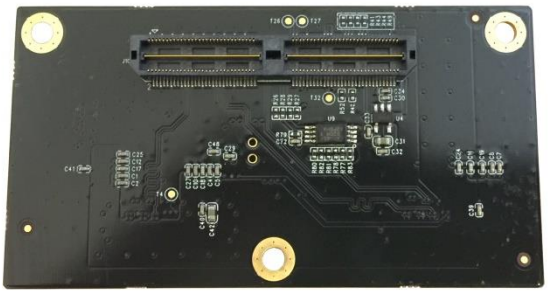
LI-JTX1-MIPI-ADPT

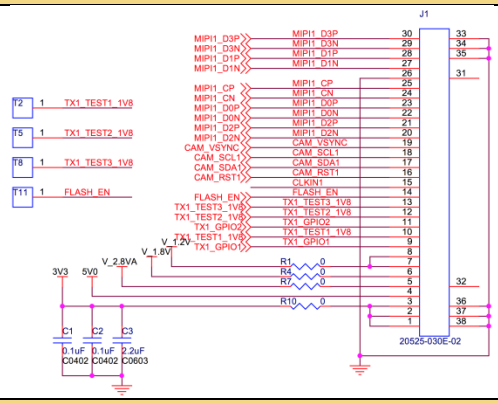




Interfaces

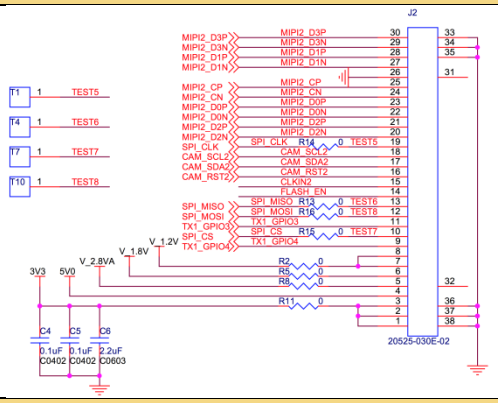
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



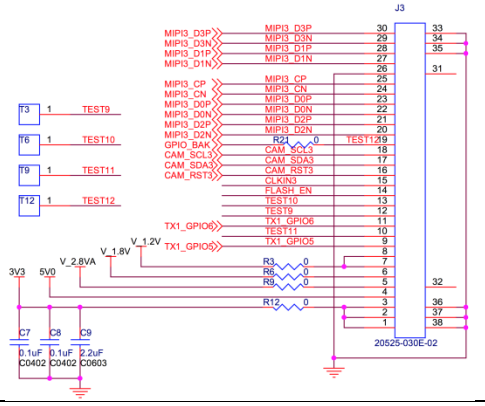
Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



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48820 Kato Rd, Suite 100B, Fremont, CA 94538, USA
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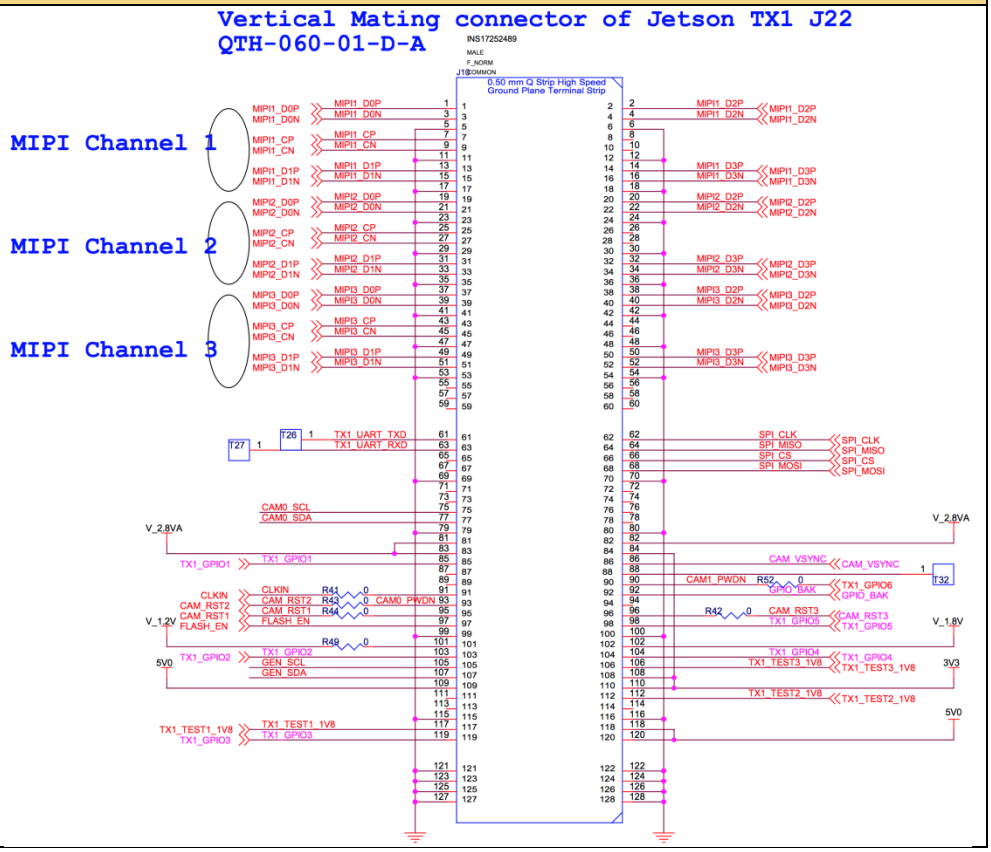
Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm



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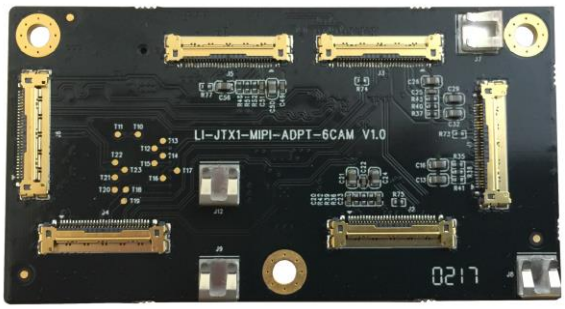
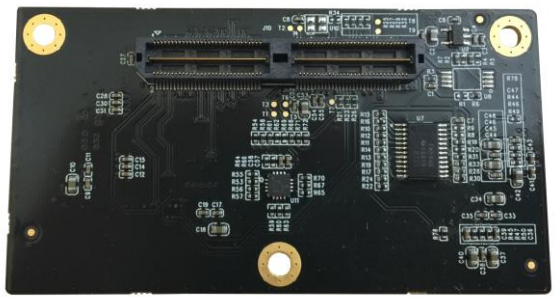
LI-JTX1-MIPI-ADPT-6CAM

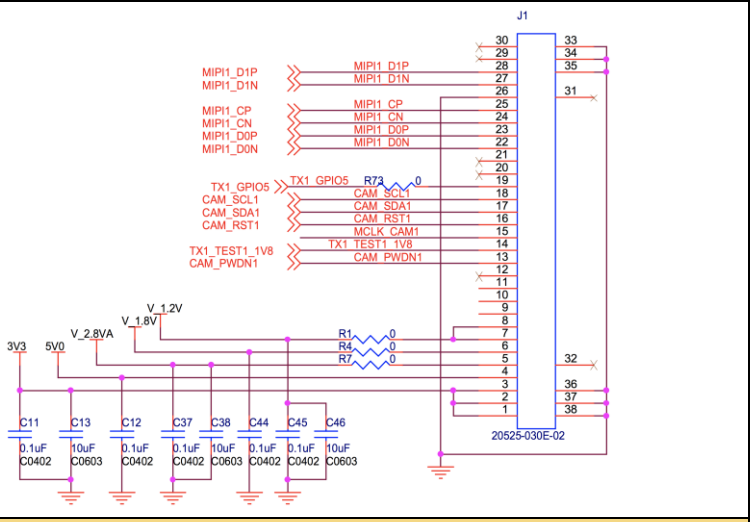




Interfaces

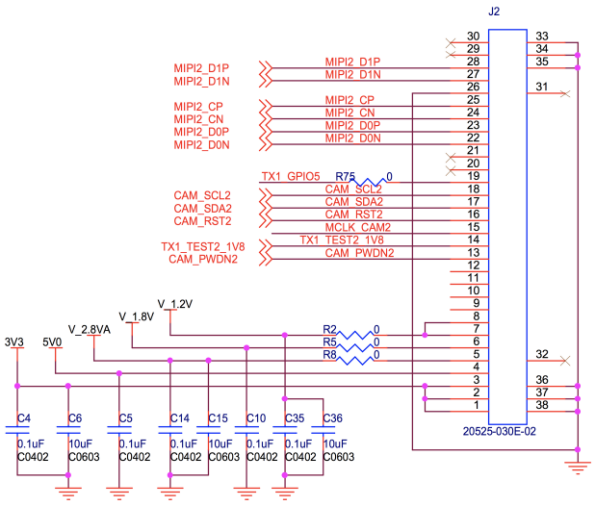
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



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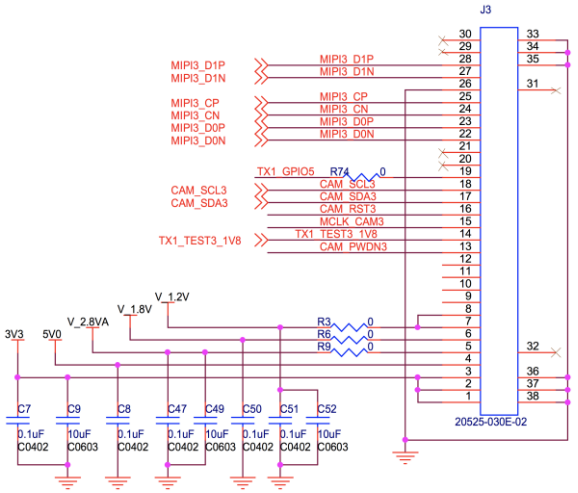
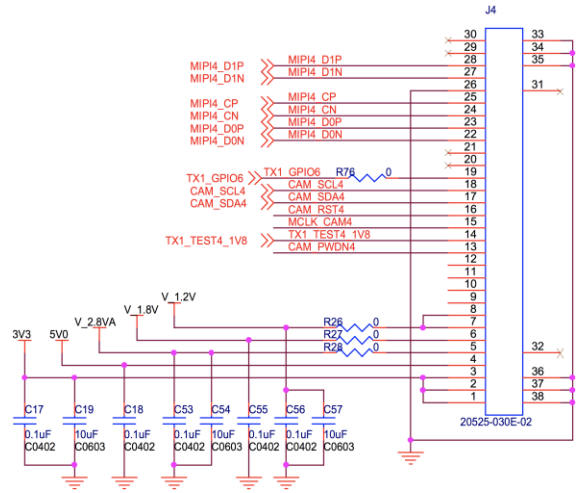
Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



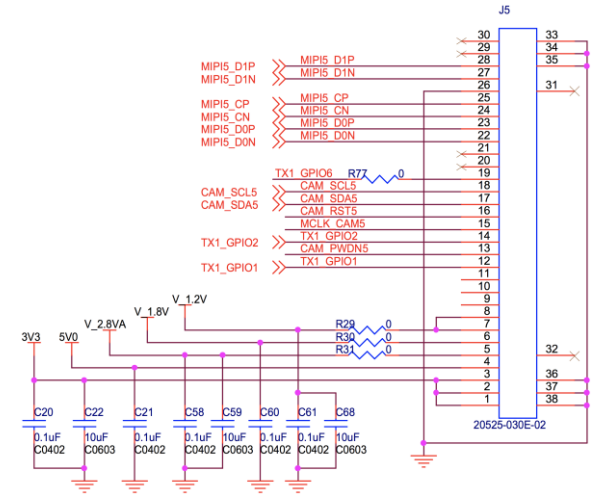
Interface J4

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J5

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
  Mating I-PEX cable: FAW-1233-03 (300mm)



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48820 Kato Rd, Suite 100B, Fremont, CA 94538, USA
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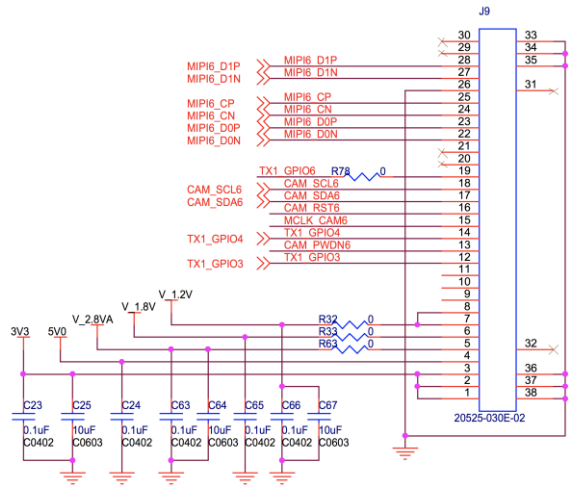
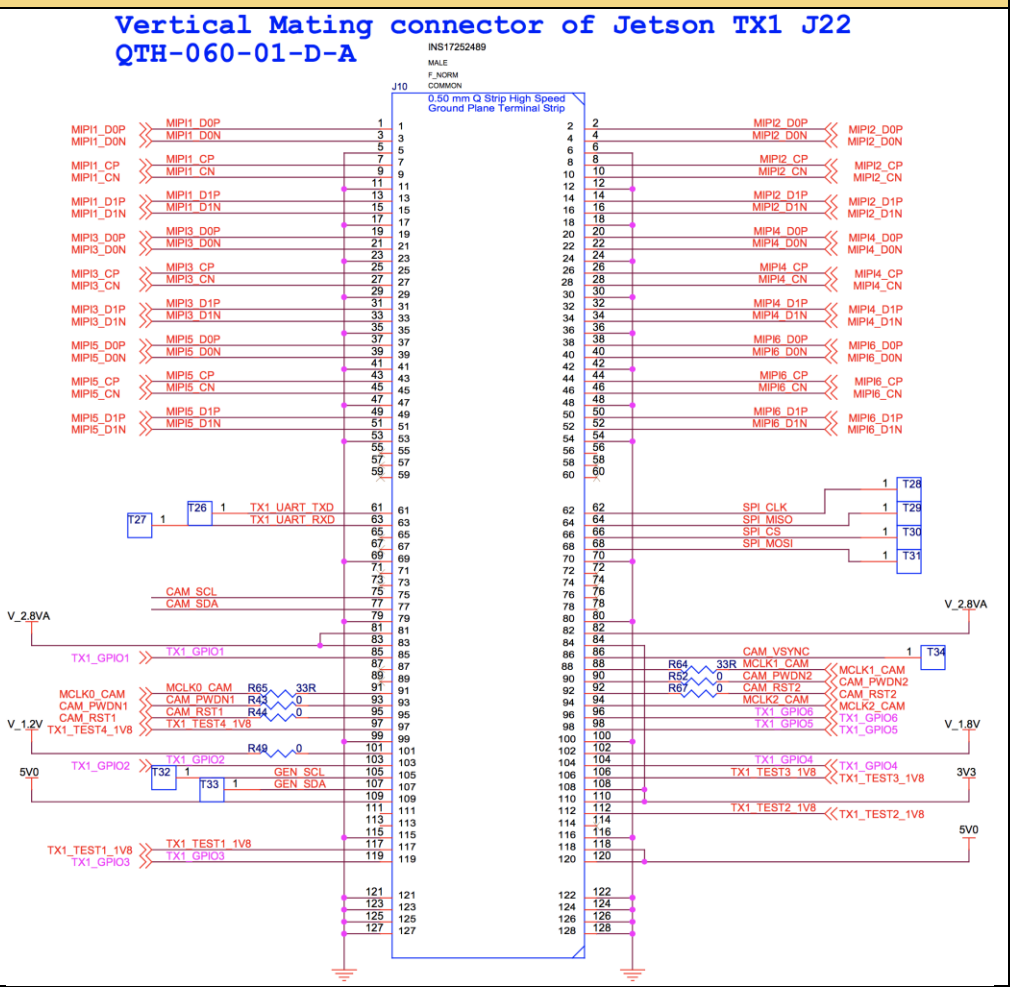
Interface J9

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
  Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm



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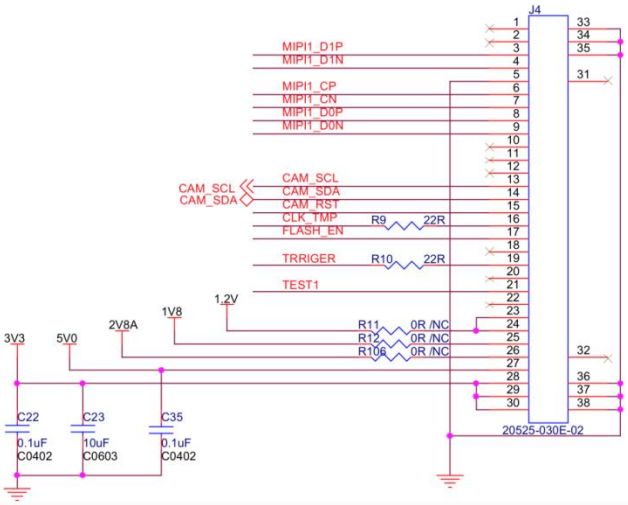
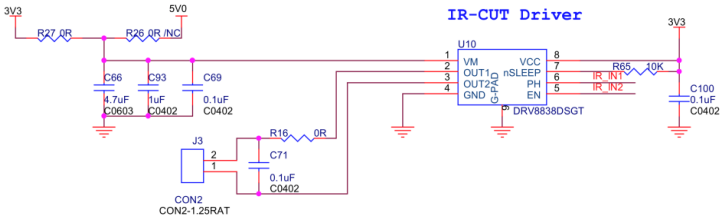
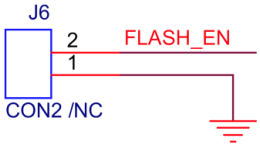
LI-AR0144-MIPI-M12

Camera Spec	
Image Sensor	ON Semiconductor CMOS Image Sensor AR0144
Optical format	1/4”
Number of active pixels	1280 (H) x 800 (V)
Pixel size	3.0um (H) x 3.0um (V)
Color or Mono	Mono
Interface	MIPI interface
Lens mount	M12
Weight	14 g
Interfaces	
Interface J2: ▪ Part#: 20525-030E-02C ▪ Number of Positions: 30 ▪ Pitch: 0.4mm ▪ Mating I-PEX cable: FAW-1233-03 (300mm)	
Interface J3: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	
Interface J5: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	

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Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.5	V	V_{SUPPLY}
I_{SUPPLY}	Total power supply current	–	200	mA	I_{SUPPLY}
I_{GND}	Total ground current	–	200	mA	I_{GND}
V_{IN}	DC input voltage	–0.3	V_{DD}_IO + 0.3	V	V_{IN}
V_{OUT}	DC output voltage	–0.3	V_{DD}_IO + 0.3	V	V_{OUT}
T_{STG}[1]	Storage temperature	–40	+125	°C	T_{STG}[1]

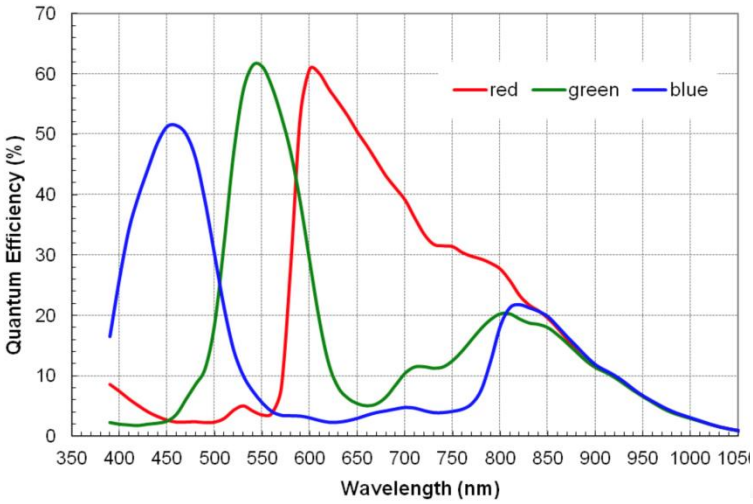
Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

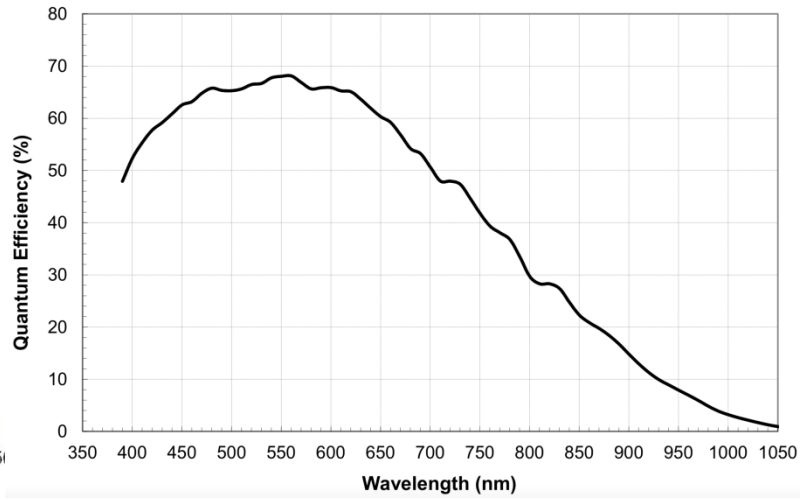
Operating Current Consumption for MIPI Output

V_{AA} = V_{AA}_PIX = V_{DD}_IO = 2.8V; V_{DD}= V_{DD}_PHY = 1.2V;PLL Enabled and PIXCLK = 74.25 MHz; T_A = 55°C; C_{LOAD} = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	MIPI, Streaming, Full resolution 60 fps	I_{DD}				mA
I/O digital operating current	MIPI, Streaming, Full resolution 60 fps	I_{DD}_IO				mA
Analog operating current	MIPI, Streaming, Full resolution 60 fps	I_{AA}				mA
Pixel supply current	MIPI, Streaming, Full resolution 60 fps	I_{AA}_PIX				mA
PLL supply current	MIPI, Streaming, Full resolution 60 fps	I_{DD}_PLL				mA
PHY supply current	MIPI, Streaming, Full resolution 60fps	I_{DD}_PHY				mA

Quantum Efficiency (Color and Mono)





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DC Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD	Core digital voltage		1.14	1.2	1.26	V
VDD_IO	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
VAA	Analog voltage		2.5	2.8	3.1	V
VAA_PIX	Pixel supply voltage		2.5	2.8	3.1	V
VDD_PHY	MIPI supply voltage		1.14	1.2	1.26	V
VIH	Input HIGH voltage		VDD_IO * 0.7	–	–	V
VIL	Input LOW voltage		–	–	VDD_IO * 0.3	V
IIN	Input leakage current	No pull-up resistor; VIN = VDD_IO or DGND	20	–	–	µA
VOH	Output HIGH voltage		VDD_IO – 0.3	–	–	V
VOL	Output LOW voltage	VDD_IO = 2.8V	–	–	0.4	V
IOH	Output HIGH current	At specified VOH	–22	–	–	mA
IOL	Output LOW current	At specified VOL	–	–	22	mA

Caution **Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

Standby Current Consumption

Analog - VAA + VAA_PIX; Digital - VDD + VDD_PHY; T_A = 55°C

Definition	Condition	Min	Typ	Max	Unit
Soft standby (clock off, driven low)	Analog, 2.8V				µA
	Digital, 1.2V				µA
	VDD_IO, 2.8V				mA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				µA
	Digital, 1.2V				mA
	VDD_IO, 2.8V				mA
Hard reset (clock off, driven low)	Analog, 2.8V				µA
	Digital, 1.2V				µA
	VDD_IO, 2.8V				mA
Hard reset (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				µA
	Digital, 1.2V				µA
	Analog, 2.8V				mA

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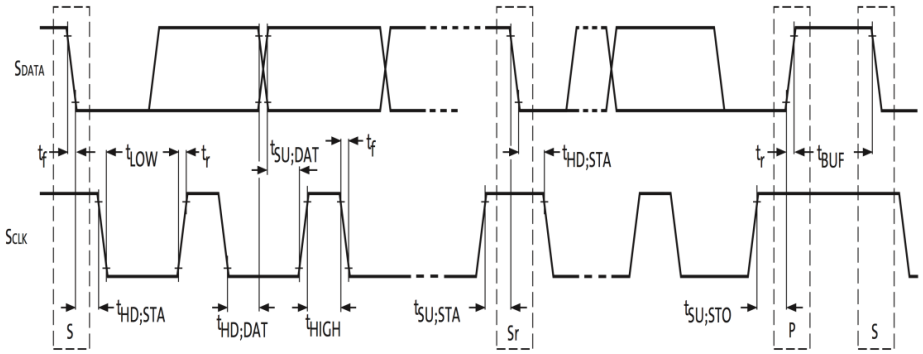
Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; VDD = 1.2V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PHY = 1.2V; T_A = 25°C

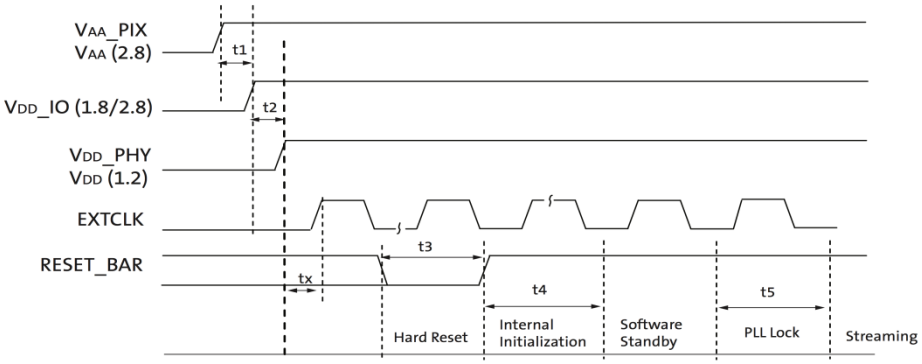
Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µS
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	µS
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	µS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µS
Data hold time:	$t_{HD;DAT}$	0[4]	3.45[5]	0[6]	0.9[5]	µS
Data set-up time	$t_{SU;DAT}$	250	-	100[6]	-	nS
Rise time of both SDATA and SCLK signals	t_r	-	1000	20 + 0.1Cb[7]	300	nS
Fall time of both SDATA and SCLK signals	t_f	-	300	20 + 0.1Cb[7]	300	nS
Set-up time for STOP condition	$tS_{U;STO}$	4.0	-	0.6	-	µS
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µS
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes:
1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I²C-compatible.
3. All values referred to V_{IHmin} = 0.9 VDD and V_{ILmax} = 0.1VDD levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

Leopard Imaging Inc.

48820 Kato Rd, Suite 100B, Fremont, CA 94538, USA
Phone: +1-408-263-0988
Fax: +1-408-217-1960
Email: sales@leopardimaging.com
Website: www.leopardimaging.com

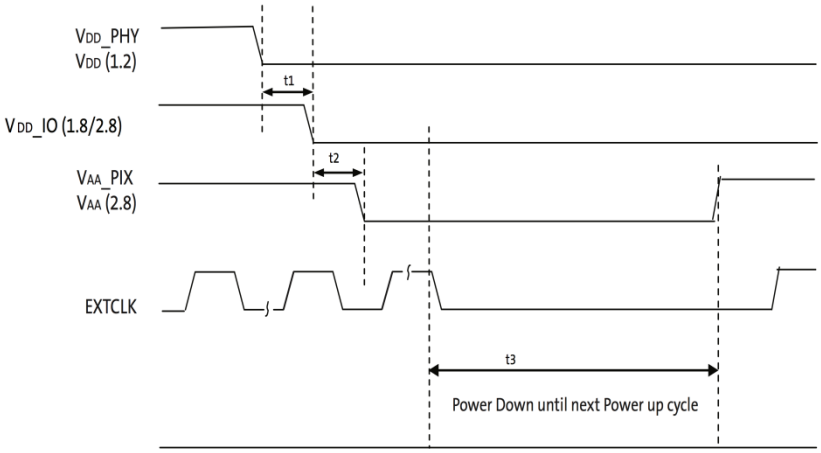
Power-on Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
VAA/VAA_PIX to VDD_IO	t1	0	10	–	µs
VDD_IO to VDD/VDD_PHY	t2	0	10	–	µs
Xtal settle time	tx	–	30[1]	–	ms
Hard Reset	t3	1[2]	–	–	ms
Internal Initialization	t4	160000	–	–	EXTCLKs
PLL Lock Time	t5	1	–	–	ms

Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PHY / VDD to VDD_IO	t1	0	–	–	µs
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µs
PwrDn until Next PwrUp Time	t3	100	–	–	ms

Note: t3 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

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