



LEOPARD IMAGING INC

Rev 1.0

LI-JETSON-KIT-AR0144CS-X

Data Sheet

Key Features

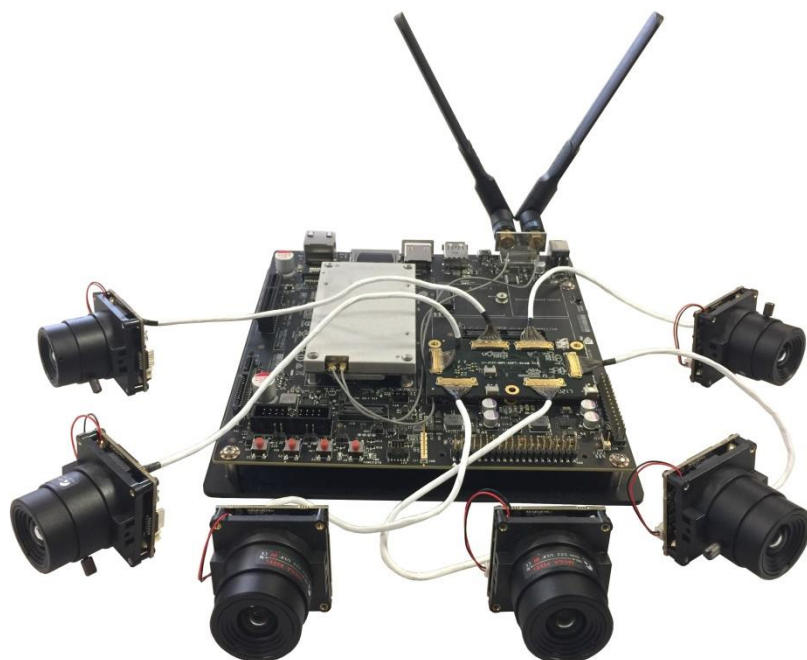
- Compatible with Nvidia Jetson TX1/TX2 Developer Kit
- MIPI CSI-2 interface
- Support up to six cameras
- Two adapter board options
 - LI-JTX1-MIPI-ADPT
Includes three 4-lane interface
 - LI-JTX1-MIPI-ADPT-6CAM
Includes six 2-lane interface
- ON Semiconductor CMOS Image Sensor AR0144
- Active pixels: 1280H x 800V
- Pixel size: 3.0 μm x 3.0 μm
- Global Shutter
- Monochrome camera
- Length of the I-PEX cable: 300mm
- Support multiple length cables
- Support IR cut switch
- Support CS lens
- Provide customization services
- Part#:

(1 cam) **LI-JETSON-KIT-AR0144CS**

(2 cam) **LI-JETSON-KIT-AR0144CS-D**

(3 cam) **LI-JETSON-KIT-AR0144CS-T**

(6 cam) **LI-JETSON-KIT-AR0144CS-H**



Lens Spec

- Model: ES0522F.IR
- Focal length: 5.0 mm
- Aperture, F/#: 2.2
- FOV (D/H/V): 56.5 °/ 50 °/28.5 °
- TV Distortion: < -8%
- Mount Type: CS

BOM

Nvidia TX1/TX2 Developer Kit not included

#	Items	QTY
1	LI-JTX1-MIPI-ADPT or LI-JTX1-MIPI-ADPT-6CAM	1
2	LI-AR0144-MIPI-CS	1,2,3 or 6
3	FAW-1233-03 cable	1,2,3 or 6



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LI-JETSON-KIT-AR0144CS

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-AR0144-MIPI-CS	1
3	FAW-1233-03 cable	1



LI-JETSON-KIT-AR0144CS-D

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-AR0144-MIPI-CS	2
3	FAW-1233-03 cable	2



LI-JETSON-KIT-AR0144CS-T

BOM

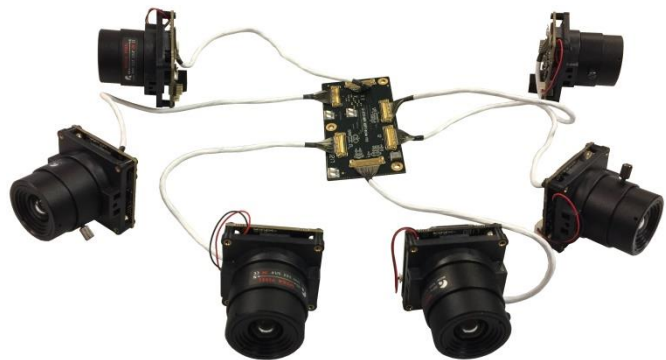
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1	LI-JTX1-MIPI-ADPT	1
2	LI-AR0144-MIPI-CS	3
3	FAW-1233-03 cable	3



LI-JETSON-KIT-AR0144CS-H

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT-6CAM	1
2	LI-AR0144-MIPI-CS	6
3	FAW-1233-03 cable	6

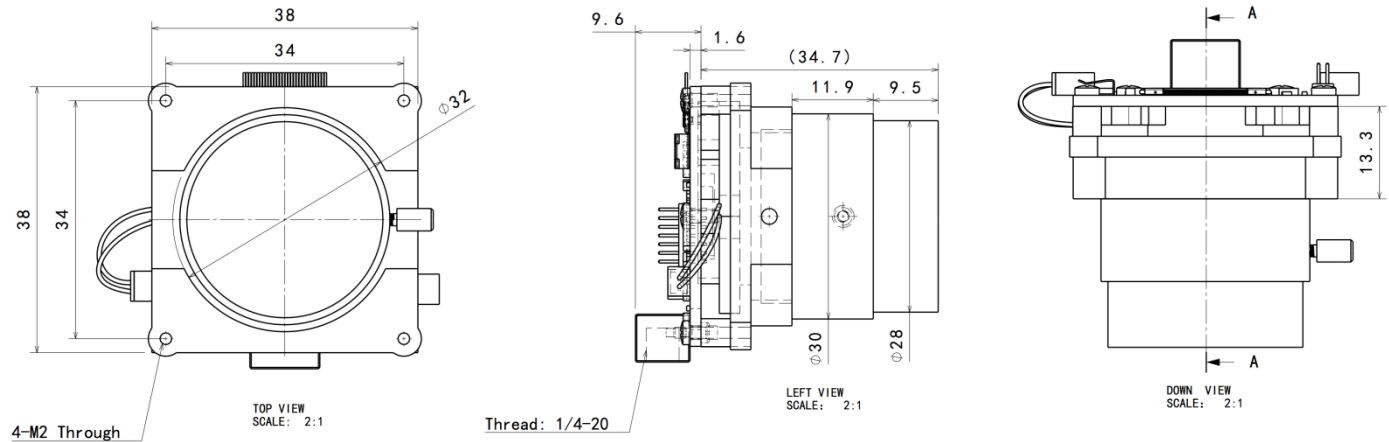


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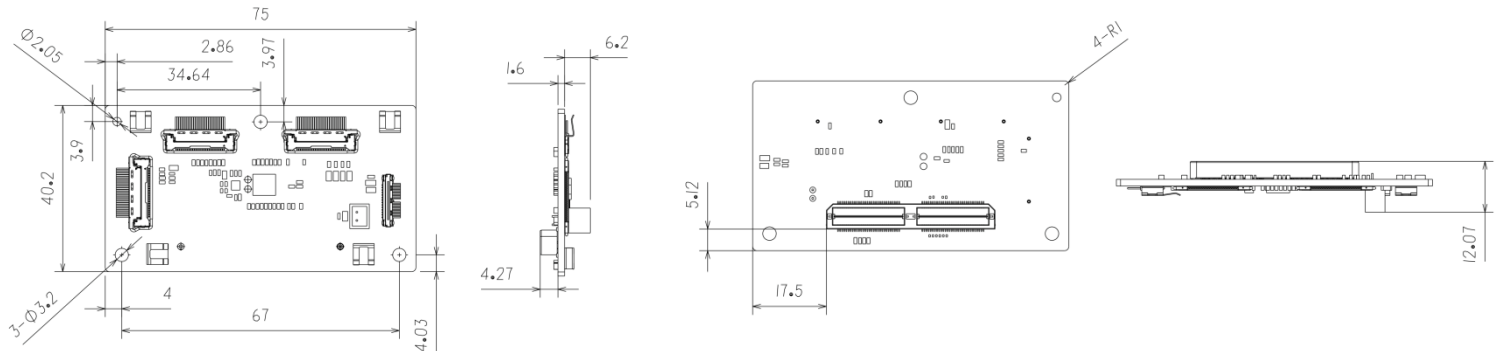
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Dimensions

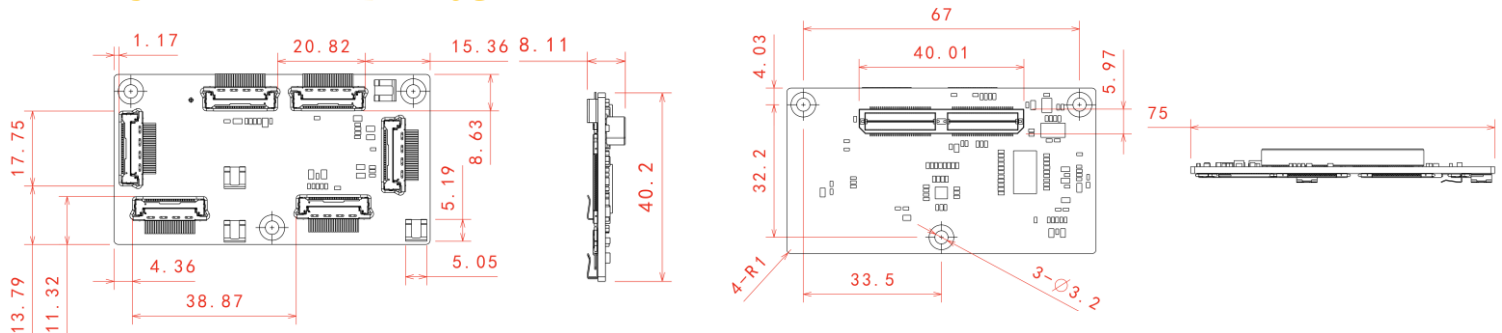
LI-AR0144-MIPI-CS



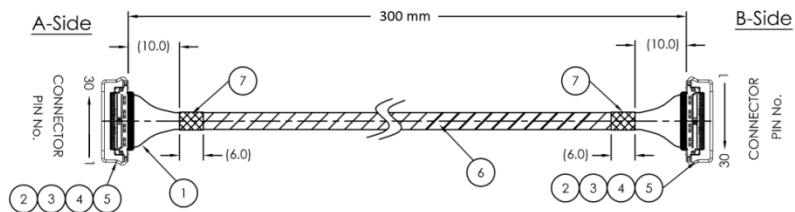
LI-JTX1-MIPI-ADPT



LI-JTX1-MIPI-ADPT-6CAM



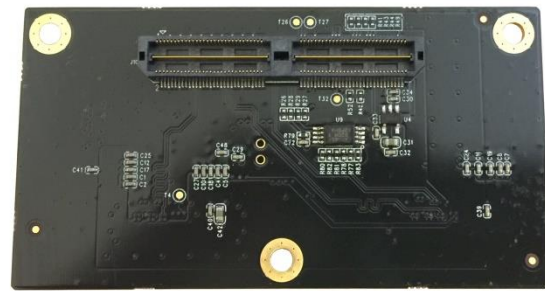
FAW-1233-03



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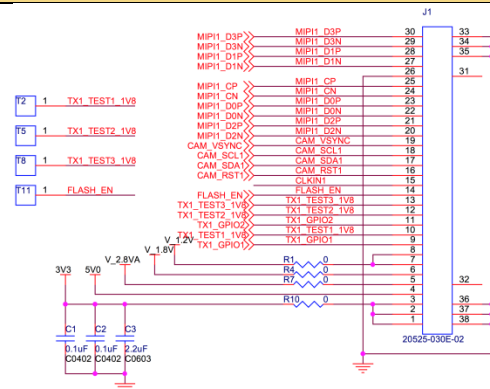
LI-JTX1-MIPI-ADPT



Interfaces

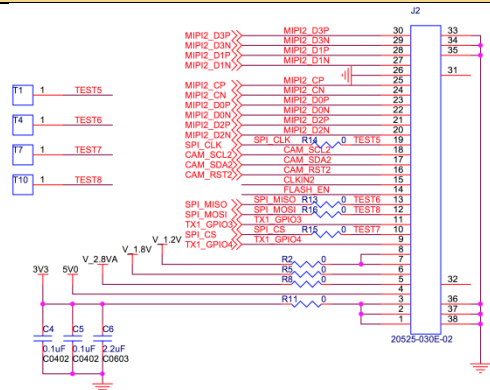
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



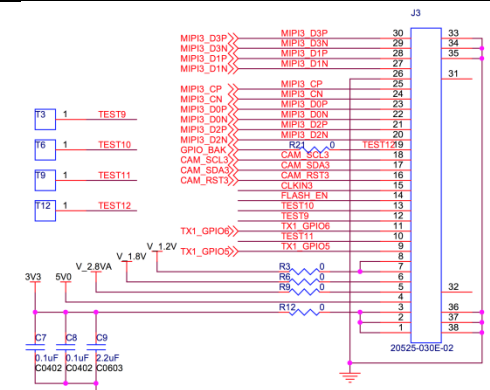
Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



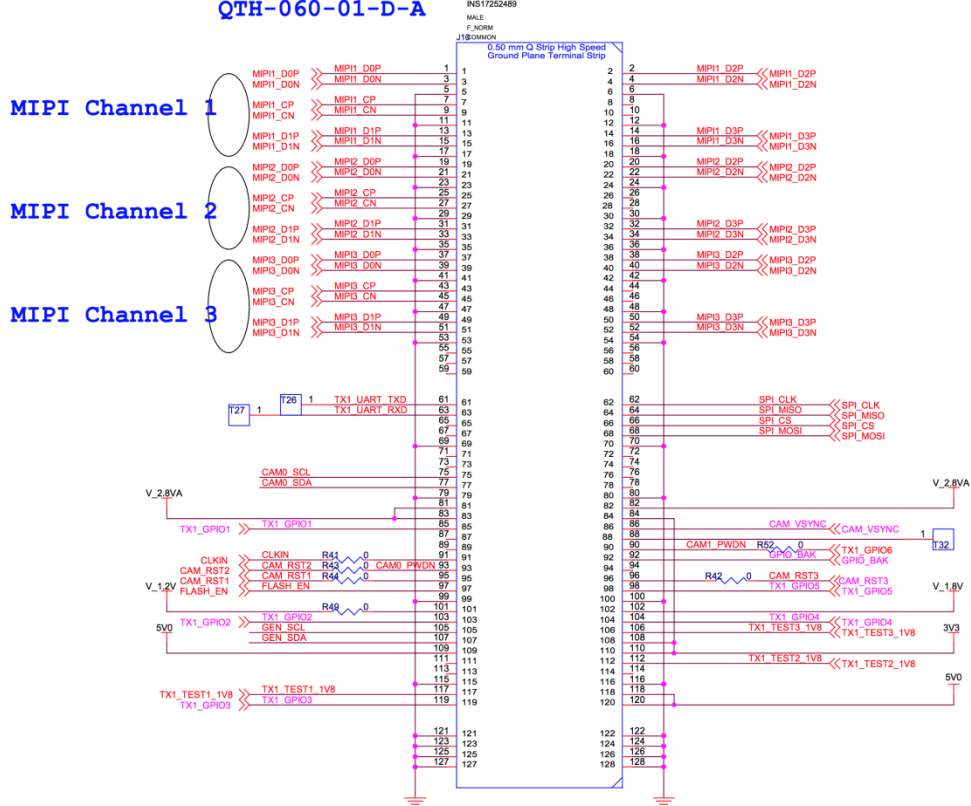
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Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm

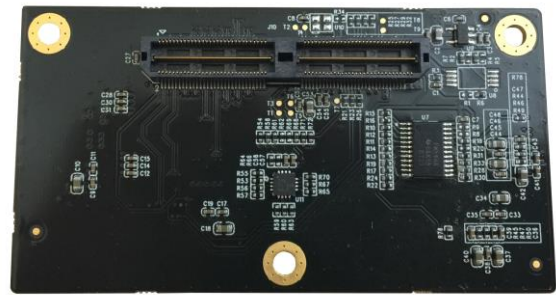
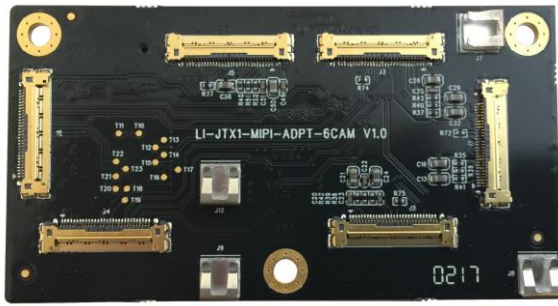
Vertical Mating connector of Jetson TX1 J22 QTH-060-01-D-A



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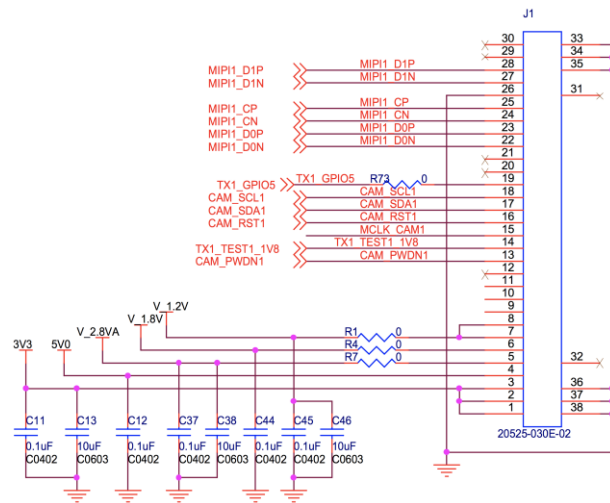
LI-JTX1-MIPI-ADPT-6CAM



Interfaces

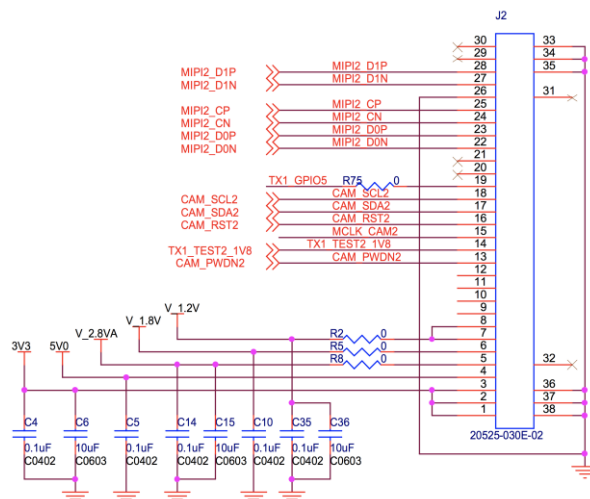
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)

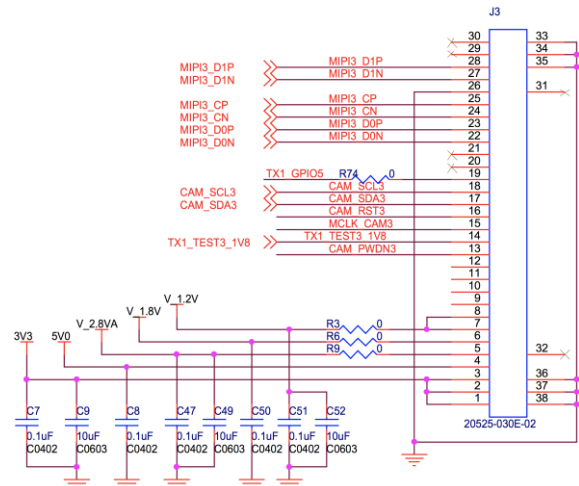


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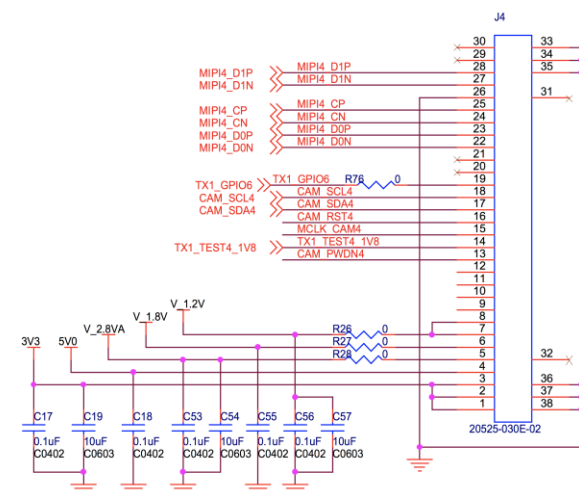
Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



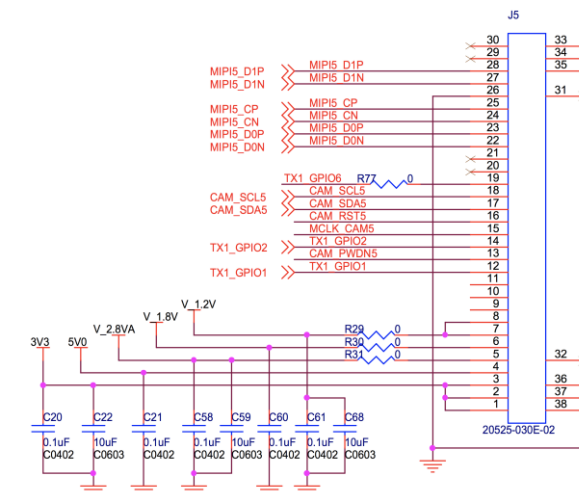
Interface J4

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J5

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)

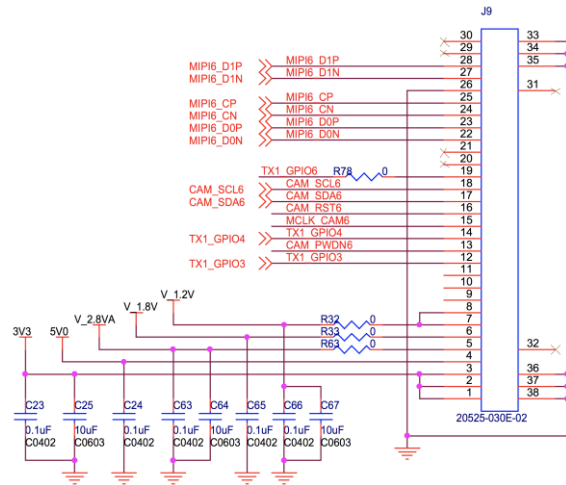


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Interface J9

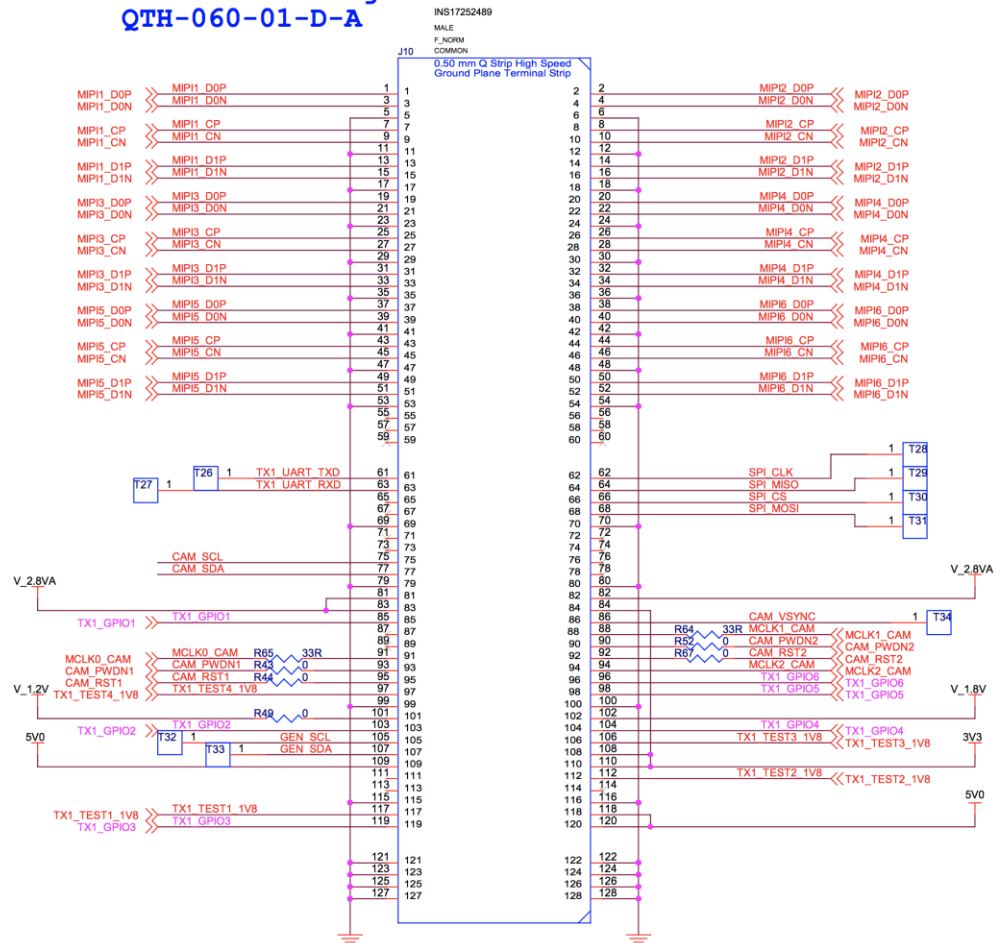
- Part#: 20525-030E-02C
 - Number of Positions: 30
 - Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm

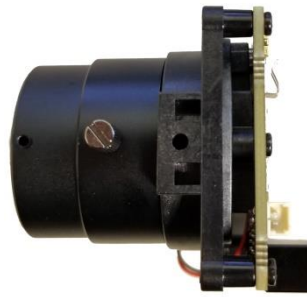
Vertical Mating connector of Jetson TX1 J22



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A black, cylindrical industrial camera module. It features a lens on the front and a connector on the side. The module is shown from a three-quarter perspective.



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Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
V _{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.5	V	V _{SUPPLY}
I _{SUPPLY}	Total power supply current	-	200	mA	I _{SUPPLY}
I _{GND}	Total ground current	-	200	mA	I _{GND}
V _{IN}	DC input voltage	-0.3	V _{DD_IO} + 0.3	V	V _{IN}
V _{OUT}	DC output voltage	-0.3	V _{DD_IO} + 0.3	V	V _{OUT}
T _{STG} ¹	Storage temperature	-40	+125	°C	T _{STG} ¹

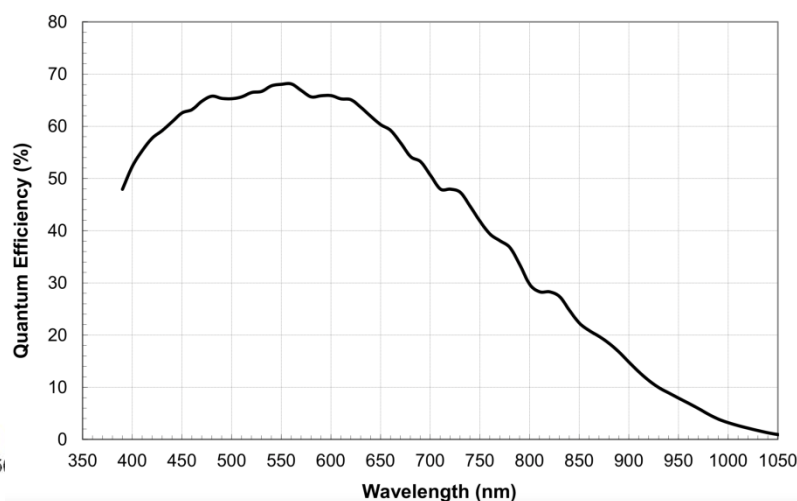
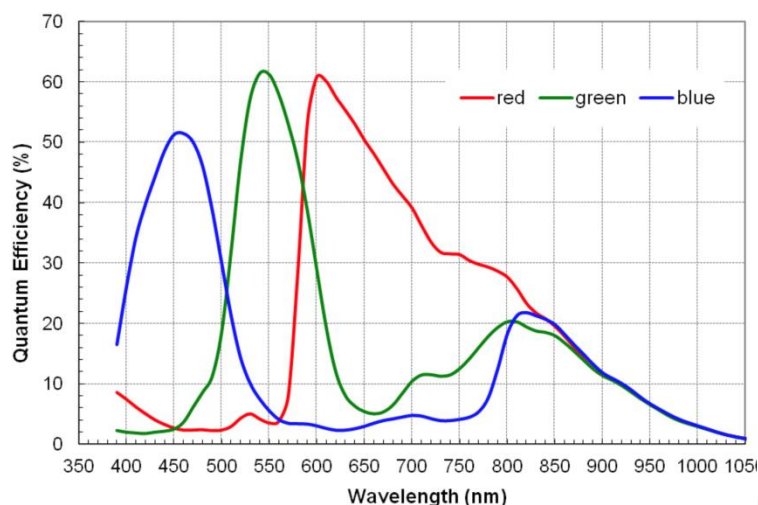
Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Current Consumption for MIPI Output

V_{AA} = V_{AA_PIX} = V_{DD_IO} = 2.8V; V_{DD} = V_{DD_PHY} = 1.2V; PLL Enabled and PIXCLK = 74.25 MHz; T_A = 55°C;
C_{LOAD} = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	MIPI, Streaming, Full resolution 60 fps	I _{DD}				mA
I/O digital operating current	MIPI, Streaming, Full resolution 60 fps	I _{DD_IO}				mA
Analog operating current	MIPI, Streaming, Full resolution 60 fps	I _{AA}				mA
Pixel supply current	MIPI, Streaming, Full resolution 60 fps	I _{AA_PIX}				mA
PLL supply current	MIPI, Streaming, Full resolution 60 fps	I _{DD_PLL}				mA
PHY supply current	MIPI, Streaming, Full resolution 60fps	I _{DD_PHY}				mA

Quantum Efficiency (Color and Mono)



DC Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD	Core digital voltage		1.14	1.2	1.26	V
VDD_IO	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
VAA	Analog voltage		2.5	2.8	3.1	V
VAA_PIX	Pixel supply voltage		2.5	2.8	3.1	V
VDD_PHY	MIPI supply voltage		1.14	1.2	1.26	V
VIH	Input HIGH voltage		VDD_IO * 0.7	–	–	V
VIL	Input LOW voltage		–	–	VDD_IO * 0.3	V
IIN	Input leakage current	No pull-up resistor; VIN = VDD_IO or DGND	20	–	–	μA
VOH	Output HIGH voltage		VDD_IO – 0.3	–	–	V
VOL	Output LOW voltage	VDD_IO = 2.8V	–	–	0.4	V
IOH	Output HIGH current	At specified VOH	–22	–	–	mA
IOL	Output LOW current	At specified VOL	–	–	22	mA

Caution Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Standby Current Consumption

Analog - VAA + VAA_PIX; Digital - VDD + VDD_PHY; TA = 55°C

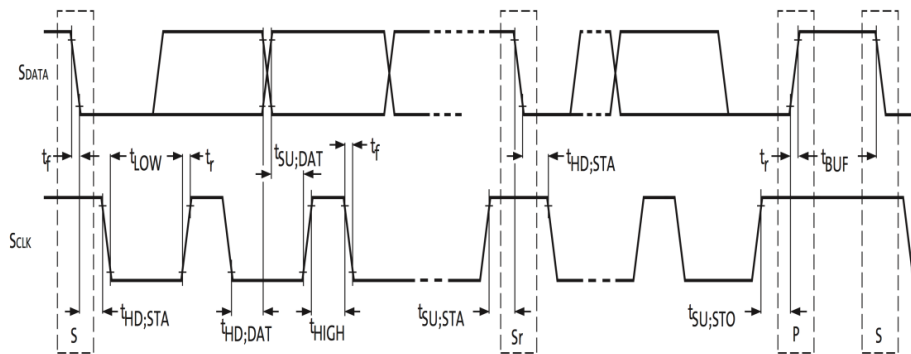
Definition	Condition	Min	Typ	Max	Unit
Soft standby (clock off, driven low)	Analog, 2.8V				μA
	Digital, 1.2V				μA
	VDD_IO, 2.8V				mA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				μA
	Digital, 1.2V				mA
	VDD_IO, 2.8V				mA
Hard reset (clock off, driven low)	Analog, 2.8V				μA
	Digital, 1.2V				μA
	VDD_IO, 2.8V				mA
Hard reset (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				μA
	Digital, 1.2V				μA
	Analog, 2.8V				mA



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Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Two-Wire Serial Bus Characteristics

$f_{EXTCLK} = 27 \text{ MHz}$; $V_{DD} = 1.2\text{V}$; $V_{DD_IO} = 2.8\text{V}$; $V_{AA} = 2.8\text{V}$; $V_{AA_PIX} = 2.8\text{V}$; $V_{DD_PHY} = 1.2\text{V}$; $T_A = 25^\circ\text{C}$

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD,STA}$	4.0	-	0.6	-	μS
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	μS
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	μS
Set-up time for a repeated START condition	$t_{SU,STA}$	4.7	-	0.6	-	μS
Data hold time:	$t_{HD,DAT}$	0 ⁴	3.45 ⁵	0 ⁶	0.9 ⁵	μS
Data set-up time	$t_{SU,DAT}$	250	-	100 ⁶	-	nS
Rise time of both SDATA and SCLK signals	t_r	-	1000	$20 + 0.1Cb^7$	300	nS
Fall time of both SDATA and SCLK signals	t_f	-	300	$20 + 0.1Cb^7$	300	nS
Set-up time for STOP condition	$t_{SU,STO}$	4.0	-	0.6	-	μS
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μS
Capacitive load for each bus line	C_b	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	K Ω

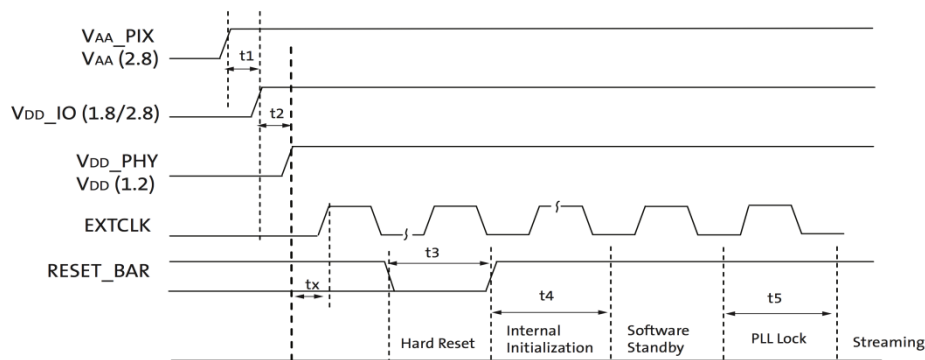
- Notes:
1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
 2. Two-wire control is I²C-compatible.
 3. All values referred to $V_{IHmin} = 0.9 V_{DD}$ and $V_{ILmax} = 0.1 V_{DD}$ levels. Sensor EXCLK = 27 MHz.
 4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
 5. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
 6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU,DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line $t_r \text{ max} + t_{SU,DAT} = 1000 + 250 = 1250 \text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCLK line is released.
 7. C_b = total capacitance of one bus line in pF.



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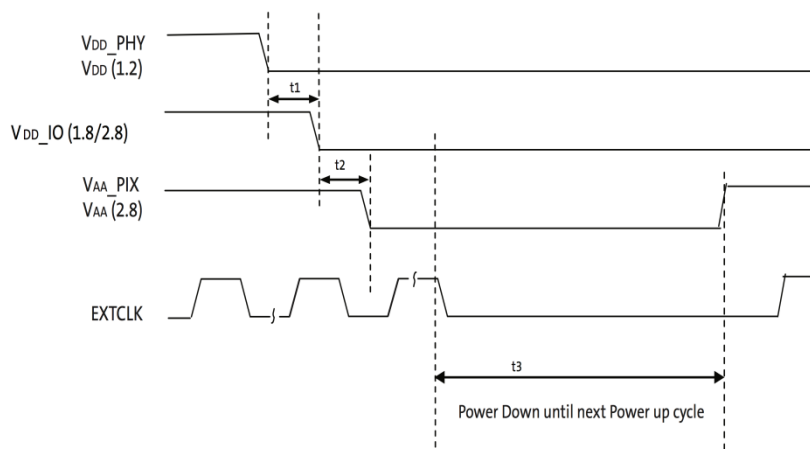
Power-on Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
VAA/VAA_PIX to VDD_IO	t_1	0	10	—	μs
VDD_IO to VDD/VDD_PHY	t_2	0	10	—	μs
Xtal settle time	t_x	—	30 ¹	—	ms
Hard Reset	t_3	1 ²	—	—	ms
Internal Initialization	t_4	160000	—	—	EXTCLKs
PLL Lock Time	t_5	1	—	—	ms

- Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
 2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PHY / VDD to VDD_IO	t_1	0	—	—	μs
VDD_IO to VAA/VAA_PIX	t_2	0	—	—	μs
PwrDn until Next PwrUp Time	t_3	100	—	—	ms

Note: t_3 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.



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