



LEOPARD IMAGING INC

LI-JETSON-CB-IMX412M12-X

Data Sheet

Key Features

- Compatible with Nvidia® Jetson™ TX1/TX2 (TX1/TX2 SOM not included)
- MIPI CSI-2 interface
- Support up to six cameras
- Two carrier board options
 - LI-TX1-CB
 - Includes three 4-lane interface
 - LI-TX1-CB-6CAM
 - Includes six 2-lane interface
- Sony Diagonal 7.857 mm (Type 1/2.3) CMOS Image Sensor IMX412
- Active pixels: 4056H x 3040V
- Pixel size: 1.55 um x 1.55 um
- Color camera
- I-PEX cable part#: FAW-1233-03
- Length of the I-PEX cable: 300mm
- Support multiple length cables
- Connector Part#: 20525-030E-02C
- Support M12 lens
- Provide customization services
- Part#:
 - (1 cam) **LI-JETSON-CB-IMX412M12**
 - (2 cam) **LI-JETSON-CB-IMX412M12-D**
 - (3 cam) **LI-JETSON-CB-IMX412M12-T**
 - (6 cam) **LI-JETSON-CB-IMX412M12-H**



Lens Spec

- Model: SYD1201A
- Focal length: 3.7 mm
- Aperture, F/#: 2.8 +/- 5%
- Built in 650nm IR cut filter
- FOV (D/H/V): 100 °/ 86 °/69 °
- TV Distortion: -1.0 %
- Mount: M12 x P0.5

BOM

Nvidia TX1/TX2 SOM not included

#	Items	QTY
1	LI-TX1-CB or LI-TX1-CB-6CAM	1
2	LI-IMX412-MIPI-M12	1,2,3 or 6
3	FAW-1233-03 cable	1,2,3 or 6
4	DC 12V power supply	1
5	USB 2.0 Type A - Micro B cable	1



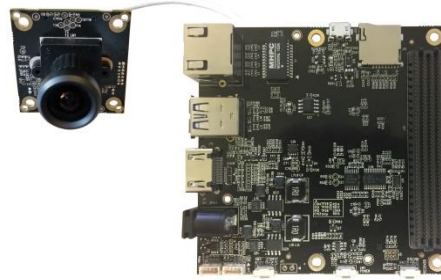
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LI-JETSON-CB-IMX412M12

BOM

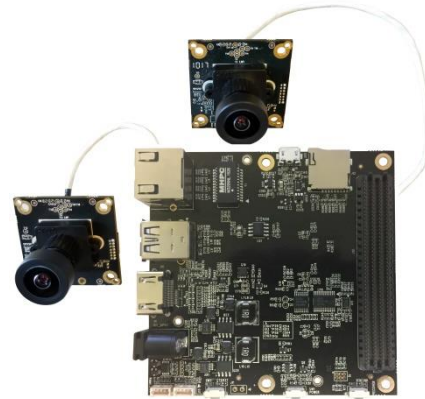
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1	LI-TX1-CB	1
2	LI-IMX412-MIPI-M12	1
3	FAW-1233-03 cable	1
4	DC 12V power supply	1
5	USB 2.0 Micro B cable	1



LI-JETSON-CB-IMX412M12-D

BOM

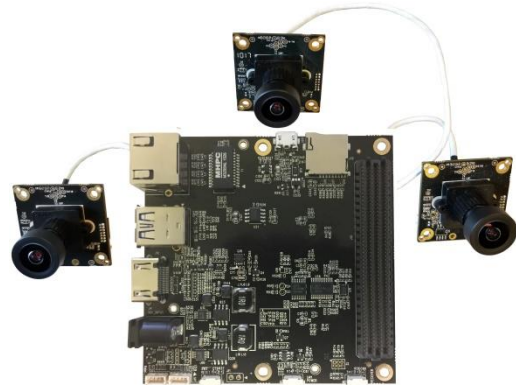
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1	LI-TX1-CB	1
2	LI-IMX412-MIPI-M12	2
3	FAW-1233-03 cable	2
4	DC 12V power supply	1
5	USB 2.0 Micro B cable	1



LI-JETSON-CB-IMX412M12-T

BOM

#	Items	QTY
1	LI-TX1-CB	1
2	LI-IMX412-MIPI-M12	3
3	FAW-1233-03 cable	3
4	DC 12V power supply	1
5	USB 2.0 Micro B cable	1



LI-JETSON-CB-IMX412M12-H

BOM

#	Items	QTY
1	LI-TX1-CB-6CAM	1
2	LI-IMX412-MIPI-M12	6
3	FAW-1233-03 cable	6
4	DC 12V power supply	1
5	USB 2.0 Micro B cable	1



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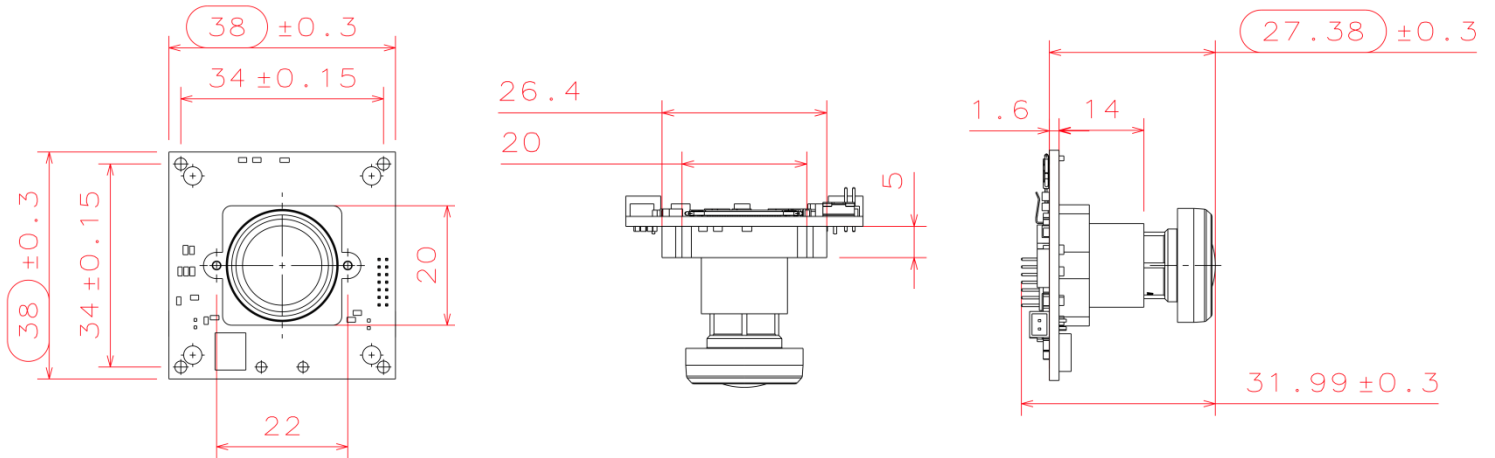
Fax: +1-408-217-1960

Email: sales@leopardimaging.com

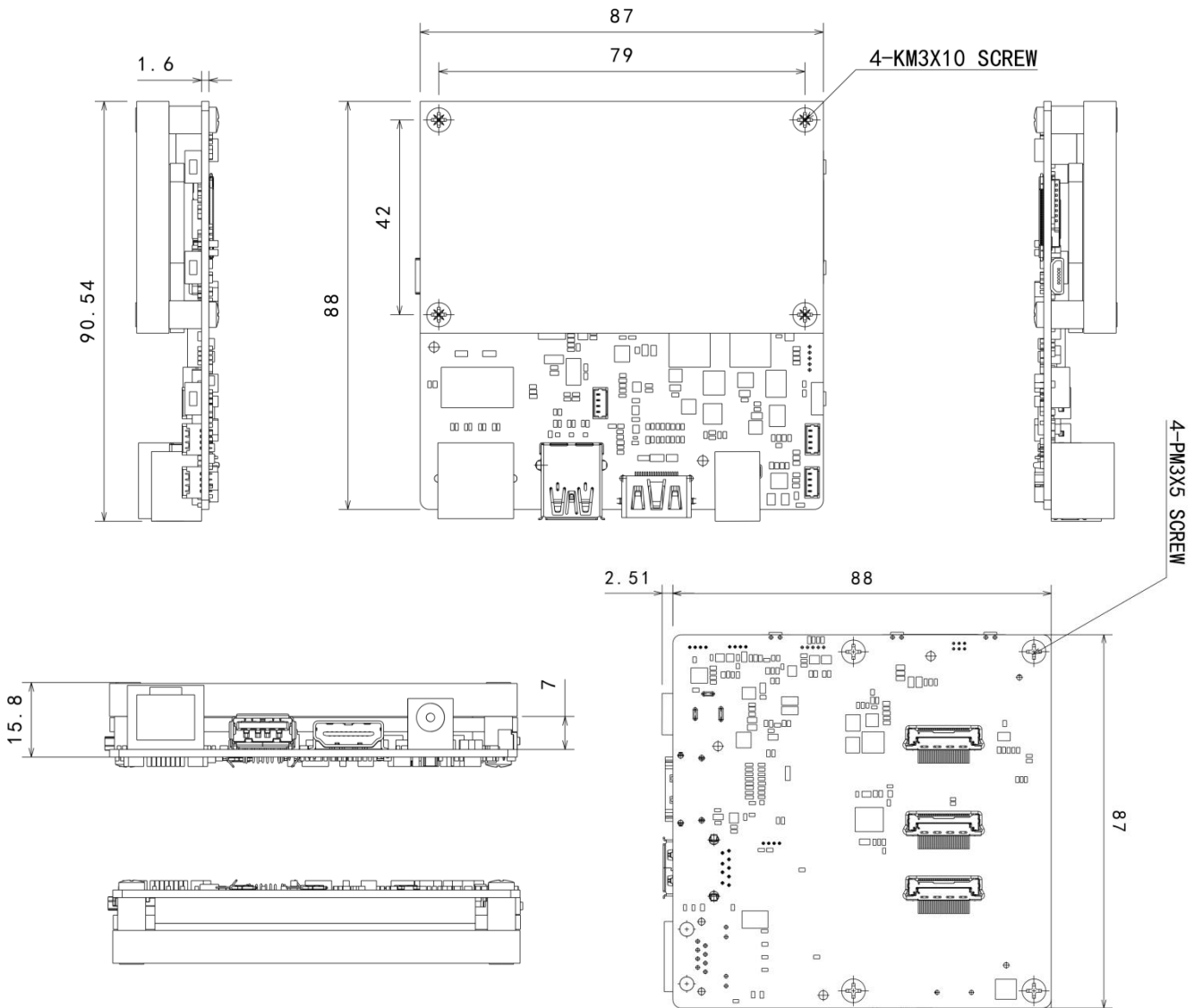
Website: www.leopardimaging.com

Dimensions

LI-IMX412-MIPI-M12



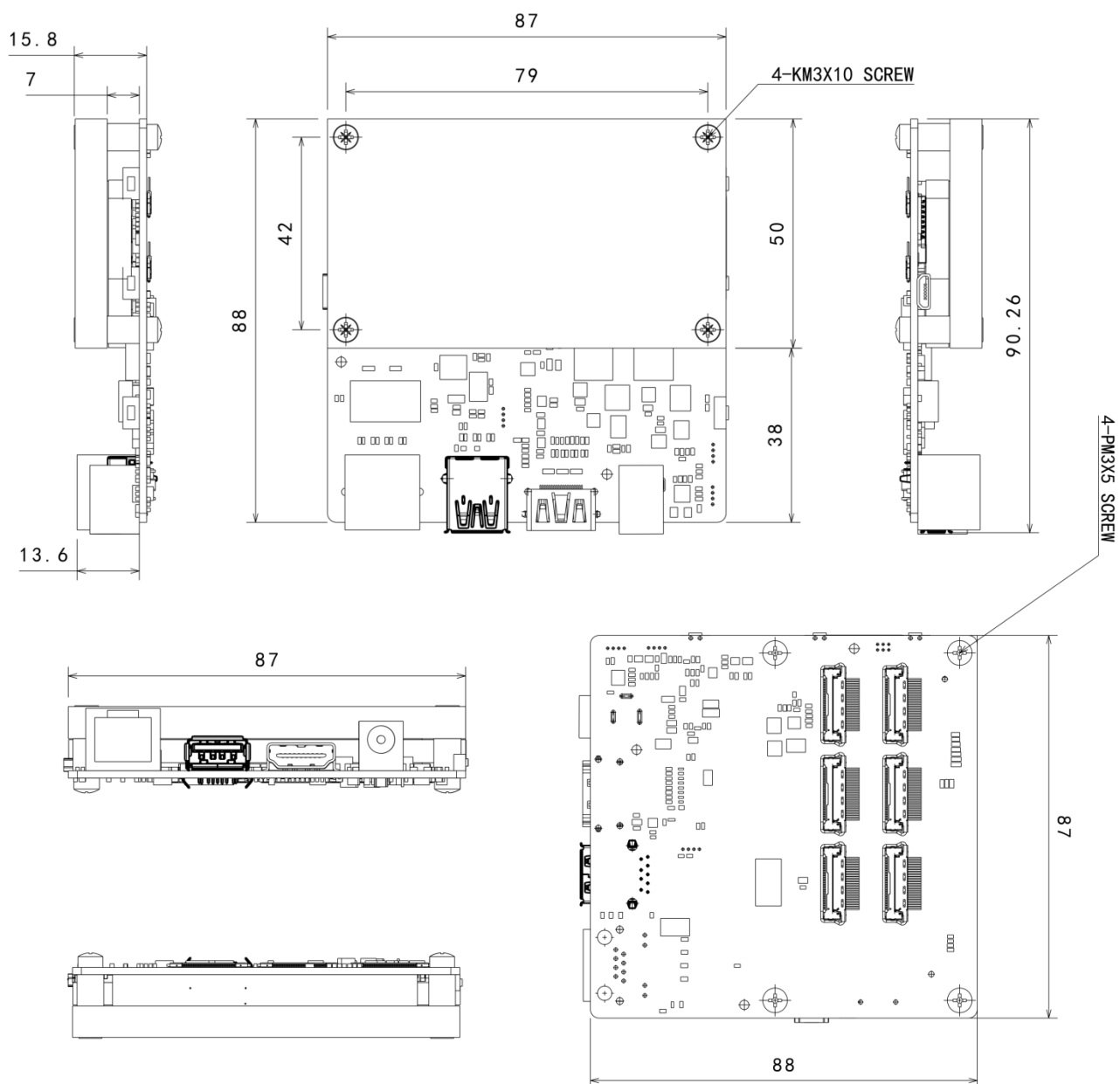
LI-TX1-CB



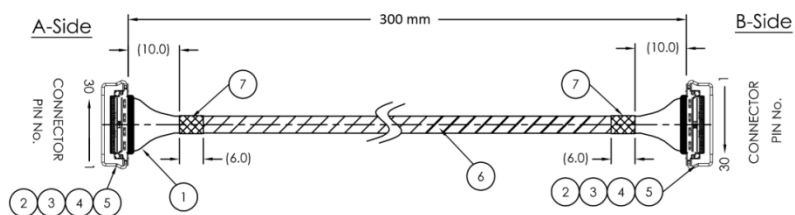
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LI-TX1-CB-6CAM

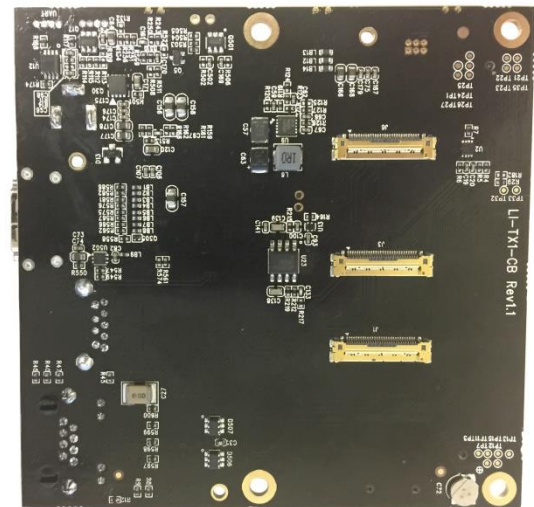
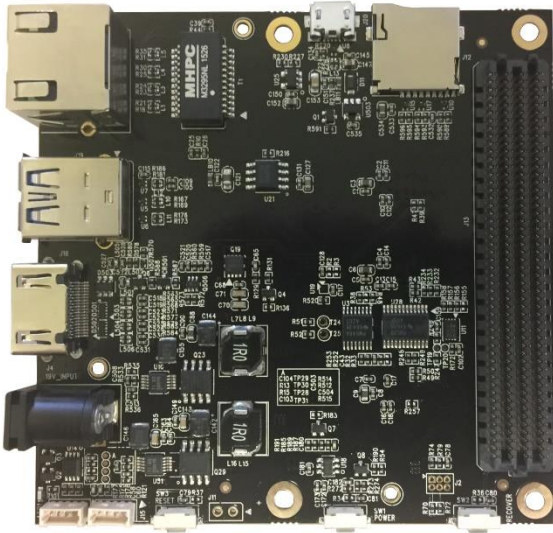


FAW-1233-03



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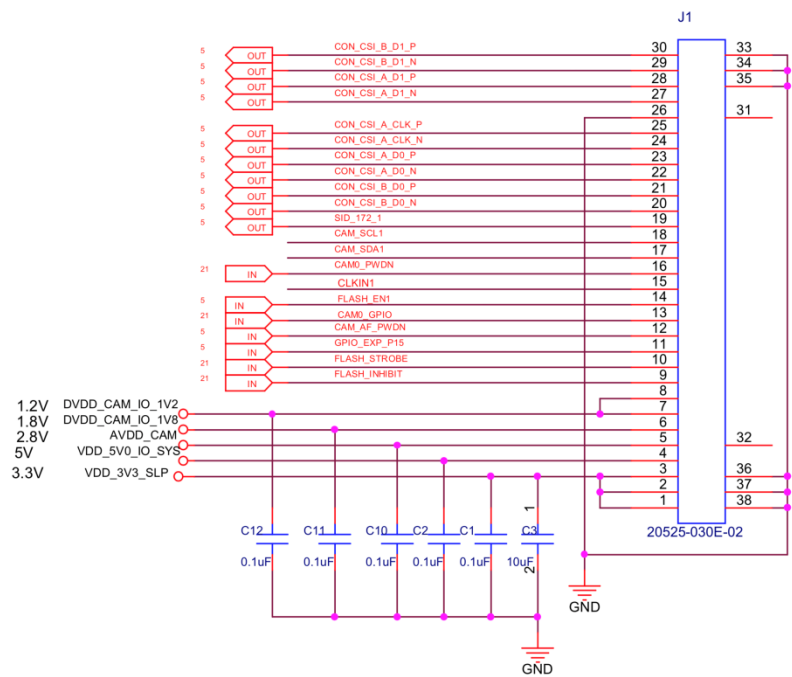
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Camera Interfaces

Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)

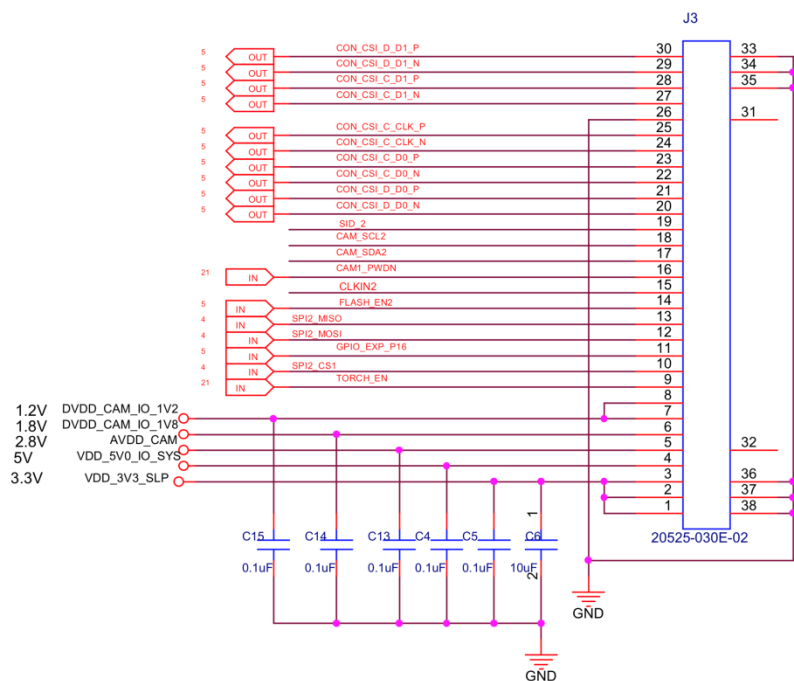


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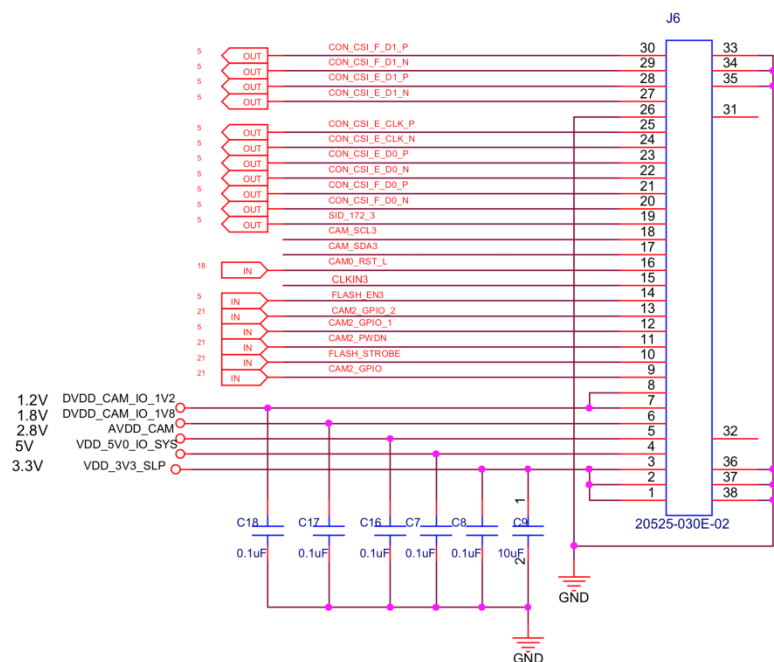
Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J6

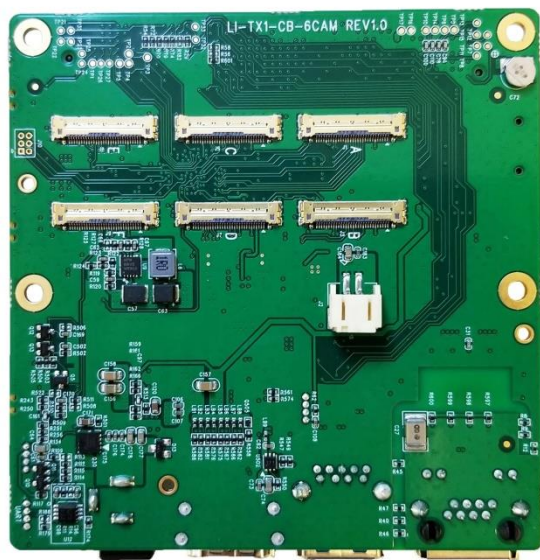
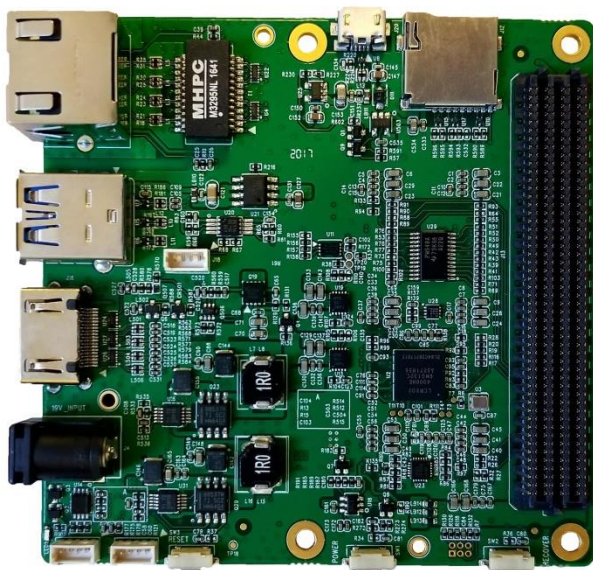
- Part#: 20525-030E-02C
 - Number of Positions: 30
 - Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



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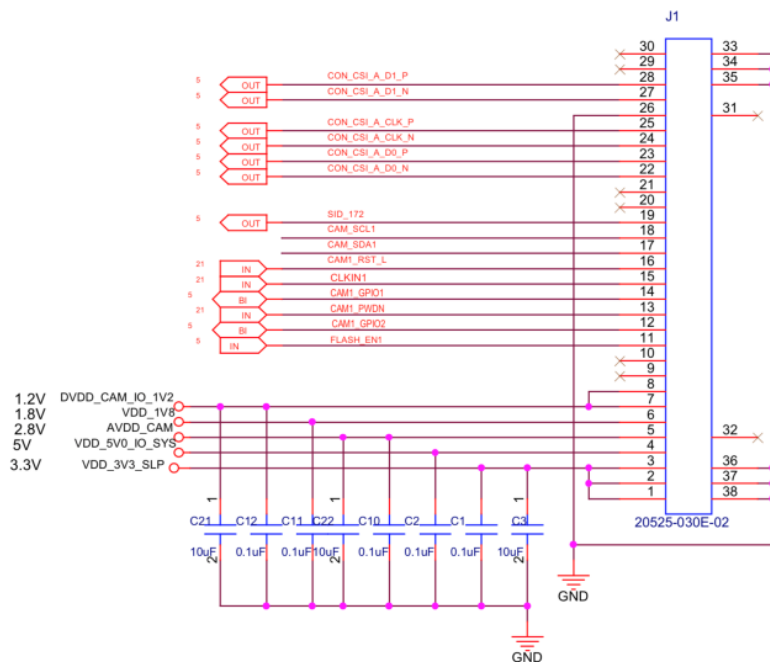
LI-TX1-CB-6CAM



Camera Interfaces

Interface J1 (camera channel A)

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable:
FAW-1233-03 (300mm)

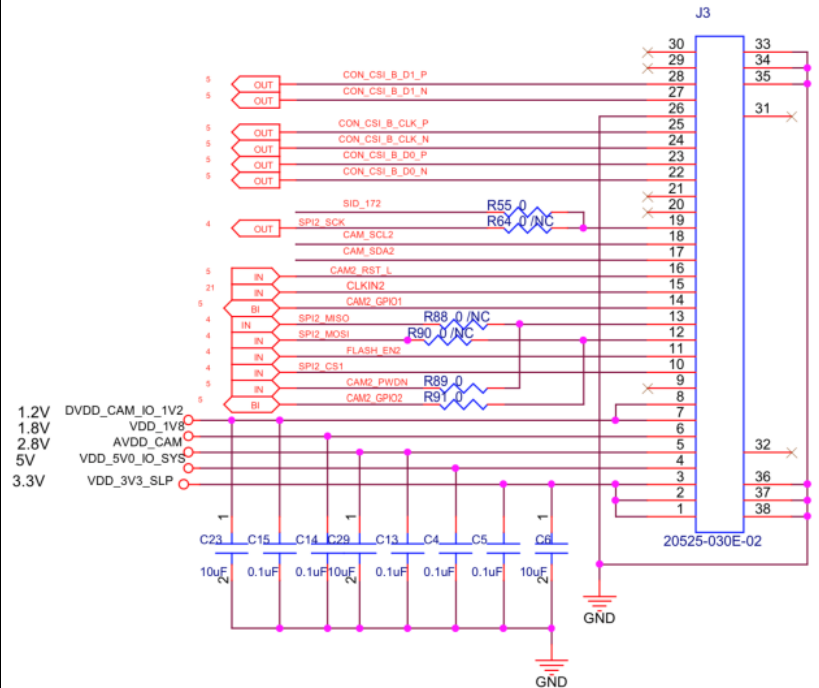


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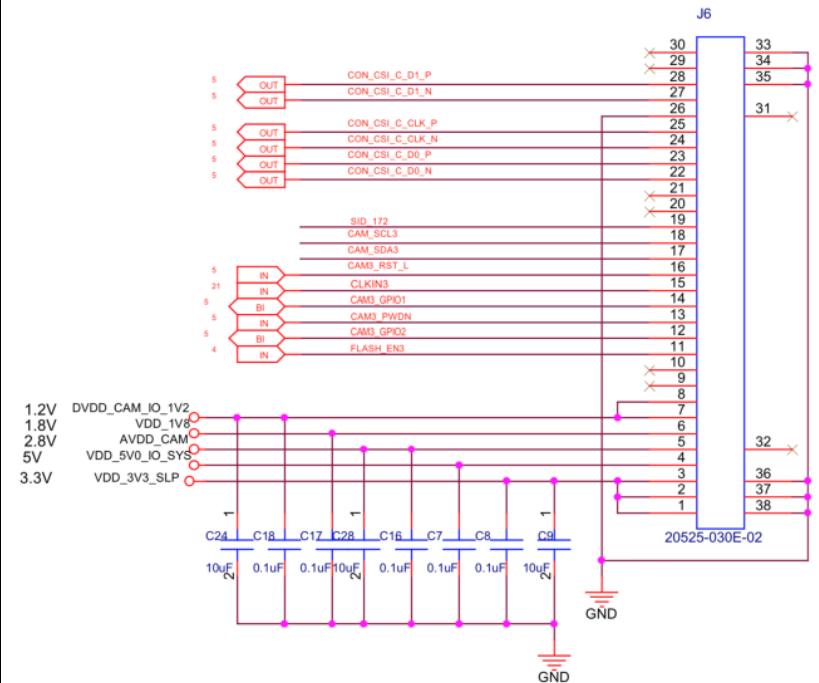
Interface J3 (camera channel B)

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable:
FAW-1233-03 (300mm)



Interface J6 (camera channel C)

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable:
FAW-1233-03 (300mm)

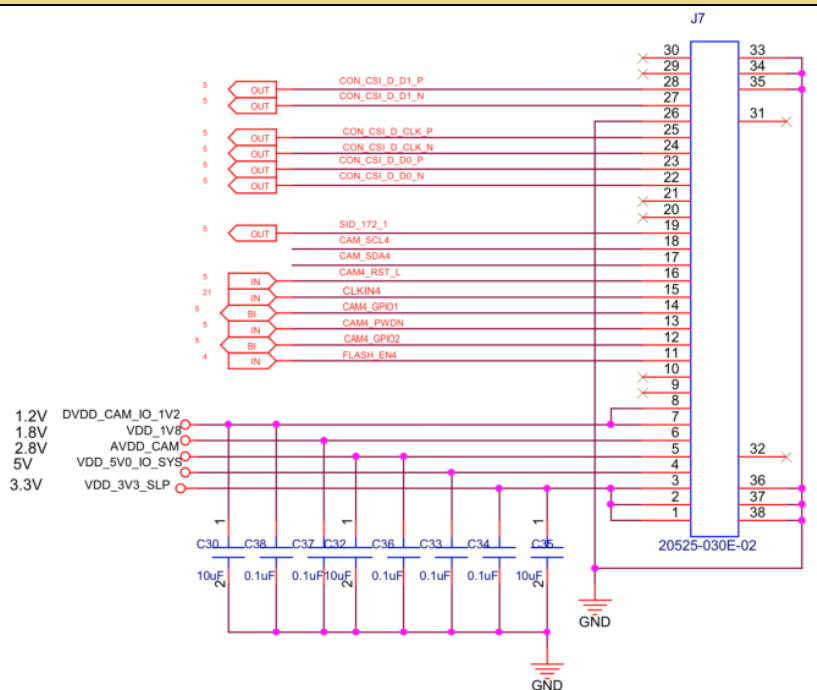


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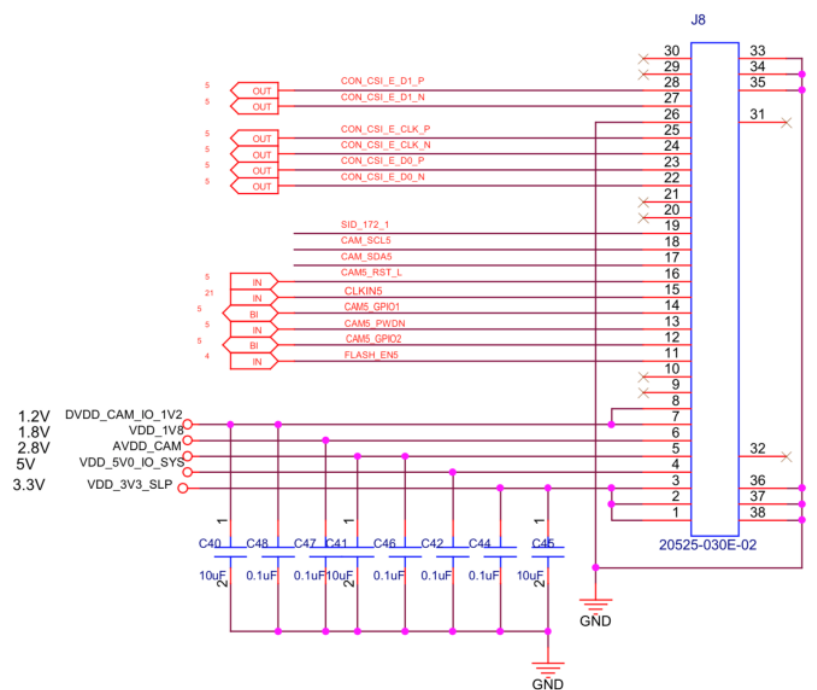
Interface J7 (camera channel D)

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable:
FAW-1233-03 (300mm)



Interface J8 (camera channel E)

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable:
FAW-1233-03 (300mm)

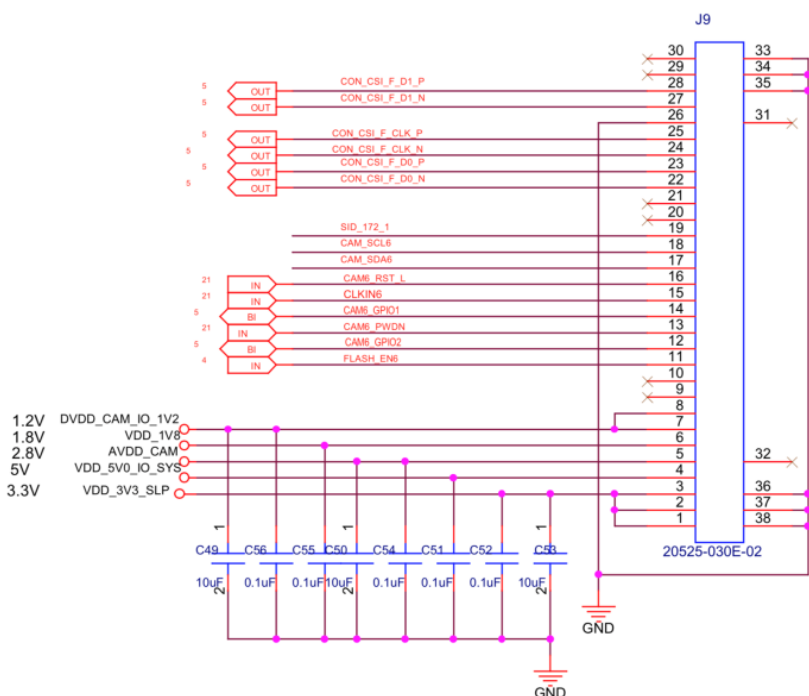


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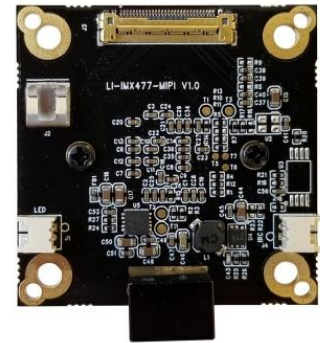
Interface J9 (camera channel F)

- Part#: 20525-030E-02C
 - Number of Positions: 30
 - Pitch: 0.4mm
- Mating I-PEX cable:
FAW-1233-03 (300mm)

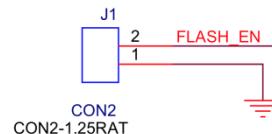
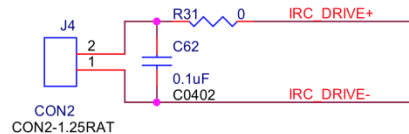
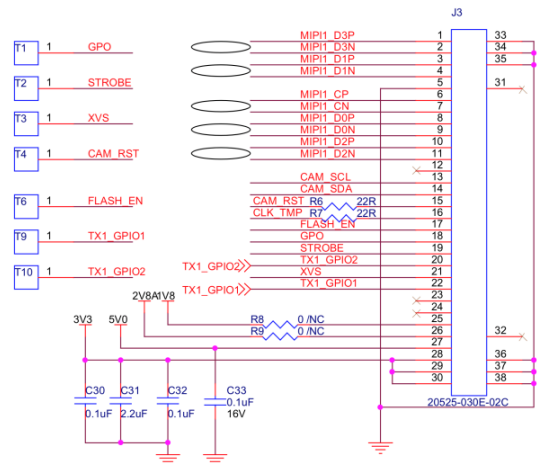


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- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Absolute Maximum Ratings

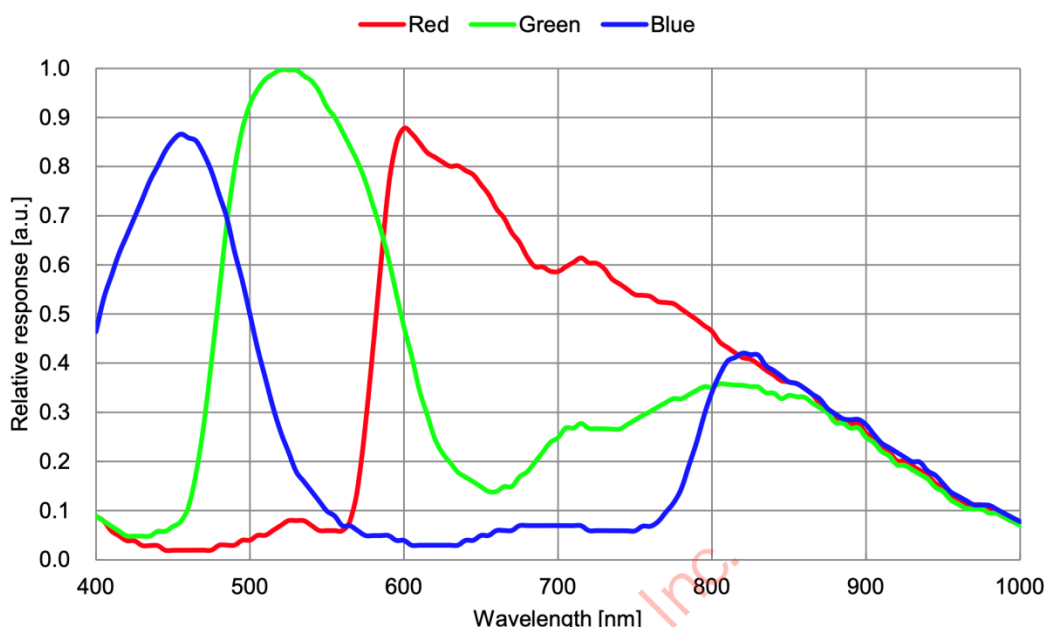
Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	V _{ANA}	-0.3 to +3.3	V	refer to V _{SS} level
Supply voltage (digital)	V _{DIG}	-0.3 to +1.8	V	
Supply voltage (interface)	V _{IF}	-0.3 to +3.3	V	
Input voltage (digital)	V _I	-0.3 to +3.3	V	
Output voltage (digital)	V _O	-0.3 to +3.3	V	
Guaranteed operating temperature	T _{OPR}	-20 to +75	°C	
Guaranteed storage temperature	T _{STG}	-30 to +80	°C	
Guaranteed performance temperature	T _{SPEC}	-20 to +60	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	V _{ANA} ^{*1}	2.8 ± 0.1	V	refer to V _{SS} level
Supply voltage (digital)	V _{DIG} ^{*2}	1.05 ± 0.1	V	
Supply voltage (interface)	V _{IF} ^{*3}	1.8 ± 0.1	V	

- ^{*1} V_{ANA}: V_{DD}SUB, V_{DD}HAN, V_{DD}HCM1 to 2, V_{DD}HSN1 to 4 (2.8 V power supply)
^{*2} V_{DIG}: V_{DD}LSC1 to 4, V_{DD}LCN1 to 2, V_{DD}LPL1 to 2, V_{DD}LIF (1.05 V power supply)
^{*3} V_{IF}: V_{DD}MIO1 to 2, V_{DD}MIF (1.8 V power supply)

Spectral Sensitivity Characteristics



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DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD} SUB, V _{DD} HCM1 to 2, V _{DD} HSN1 to 4, V _{DD} HAN	V _{ANA}		2.7	2.8	2.9	V
	V _{DD} LCN1 to 2, V _{DD} LSC1 to 4, V _{DD} LIF, V _{DD} LPL1 to 2	V _{DIG}		0.95	1.05	1.15	V
	V _{DD} MIO1 to 2, V _{DD} MIF	V _{IF}		1.7	1.8	1.9	V
Digital input voltage	SDA,	V _{IH}		0.7 V _{IF}		2.9	V
	SCL	V _{IL}		- 0.3		0.3 V _{IF}	V
Digital input voltage	XCLR, INCK, SLASEL	V _{IH}		0.65 V _{IF}		V _{IF} + 0.3	V
		V _{IL}		- 0.3		0.35 V _{IF}	V
Digital output voltage	SDA	V _{OH}		V _{IF} - 0.4			V
		V _{OL}				0.4	V
Digital output voltage	GPO	V _{OH}		V _{IF} - 0.4			V
		V _{OL}				0.4	V



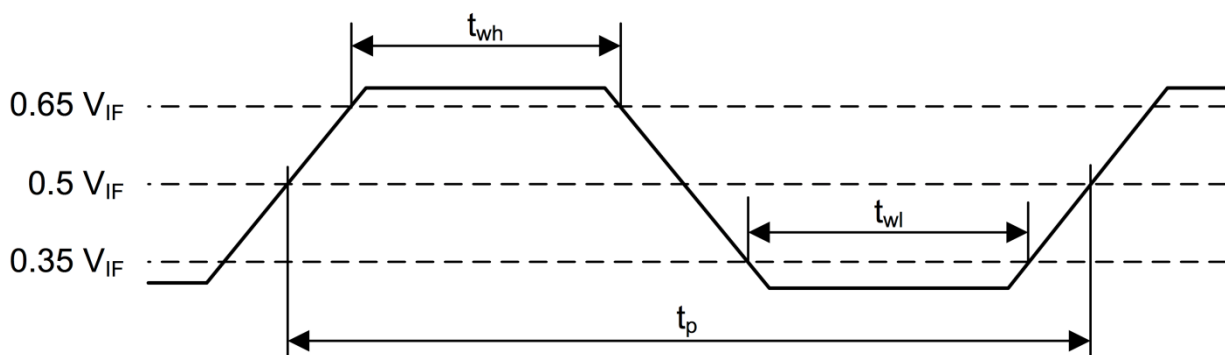
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AC Characteristics

Master Clock Square Waveform Input Diagram

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.



Master Clock Square Waveform Input Characteristics

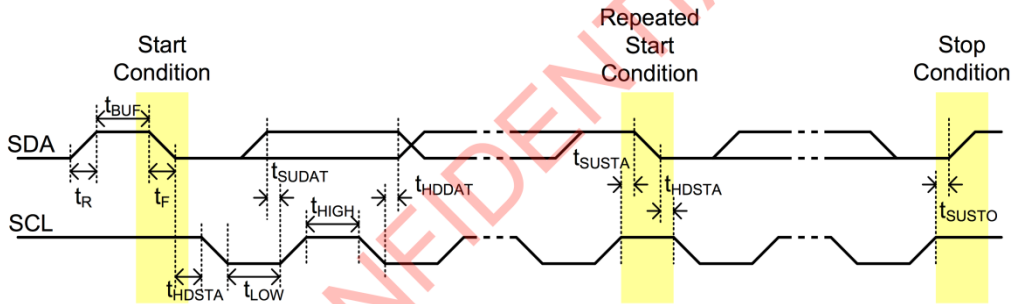
PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f _{SCK}	6		27	MHz
INCK clock period	t _p	37.0		166.7	ns
INCK low level width	t _{wl}	0.4 t _p		0.6 t _p	ns
INCK high level width	t _{wh}	0.4 t _p		0.6 t _p	ns
INCK jitter	T _{jitter}			600	ps



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2-wire serial communication block characteristics



2-wire serial communication block specification

Parameter	Symbol	Conditions	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
Low level input voltage	V_{IL}		-0.5	0.3 V_{IF}	V
High level input voltage	V_{IH}		0.7 V_{IF}	2.9	V
Low level output voltage	V_{OL1}	$V_{IF} > 2$ V, Sink 3 mA	0	0.4	V
	V_{OL2}	$V_{IF} < 2$ V, Sink 3 mA	0	0.2 V_{IF}	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 $V_{IF} \rightarrow$ 0.3 V_{IF}		250 (120)	ns
Input current	I_I	0.1 $V_{IF} \rightarrow$ 0.9 V_{IF}	-10	10	μ A
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	C_I			10	pF

2-wire serial communication block AC specification

Parameter	Symbol	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
SCL clock frequency	f_{SCL}	0	400 (1000)	kHz
Rise time (SDA and SCL)	t_R	—	300 (120)	ns
Fall time (SDA and SCL)	t_F	—	300 (120)	ns
Hold time (start condition)	t_{HDSTA}	0.6 (0.26)	—	μ s
Setup time (rep.-start condition)	t_{SUSTA}	0.6 (0.26)	—	μ s
Setup time (stop condition)	t_{SUSTO}	0.6 (0.26)	—	μ s
Data setup time	t_{SUDAT}	100 (50)	—	ns
Data hold time	t_{HDDAT}	0	—	μ s
Bus free time between Stop and Start condition	t_{BUF}	1.3 (0.5)	—	μ s
Low period of the SCL clock	t_{LOW}	1.3 (0.5)	—	μ s
High period of the SCL clock	t_{HIGH}	0.6 (0.26)	—	μ s

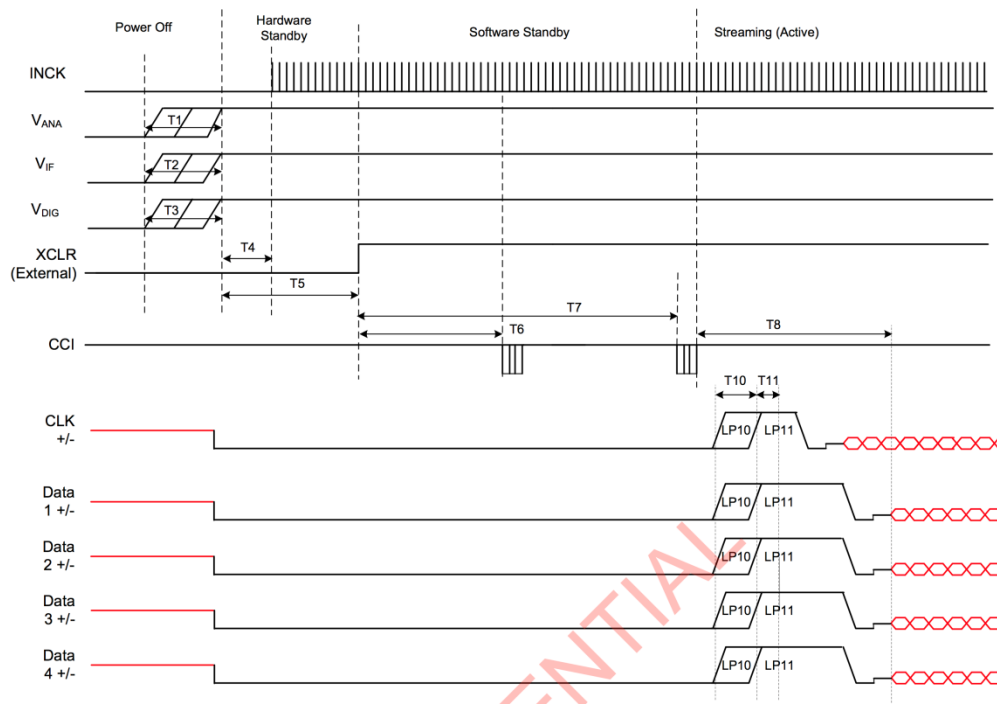
Note) Fast-mode Plus supports only available with INCK $\geq$ 8.0 MHz



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Power-on Sequence



Item	Label	Min.	Max.	Unit	Comment
V_{ANA} rising – V_{ANA} ON	T1	V_{ANA} and V_{IF} and V_{DIG} may rise in any order.		μs	Slew rate of V_{ANA} , V_{IF} and V_{DIG} (0 % - 100 %): Max. 50 mV/ μs
V_{IF} rising – V_{IF} ON	T2			μs	
V_{DIG} rising – V_{DIG} ON	T3			μs	
V_{ANA} and V_{IF} and V_{DIG} rising - INCK start	T4	0		μs	Presence of INCK during Power off is acceptable
V_{ANA} and V_{IF} and V_{DIG} rising - XCLR rising	T5	0		ms	After T1,T2 and T3
INCK start and XCLR rising till CCI Read version ID register wait time	T6	0.6		ms	
INCK start and XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	8		ms	
Start of first streaming from Sending Streaming Command.	T8		4.0 ms + The delay of the coarse integration time value		
D-PHY power up	T10	1	1.1	ms	
D-PHY init.	T11	100	110	μs	

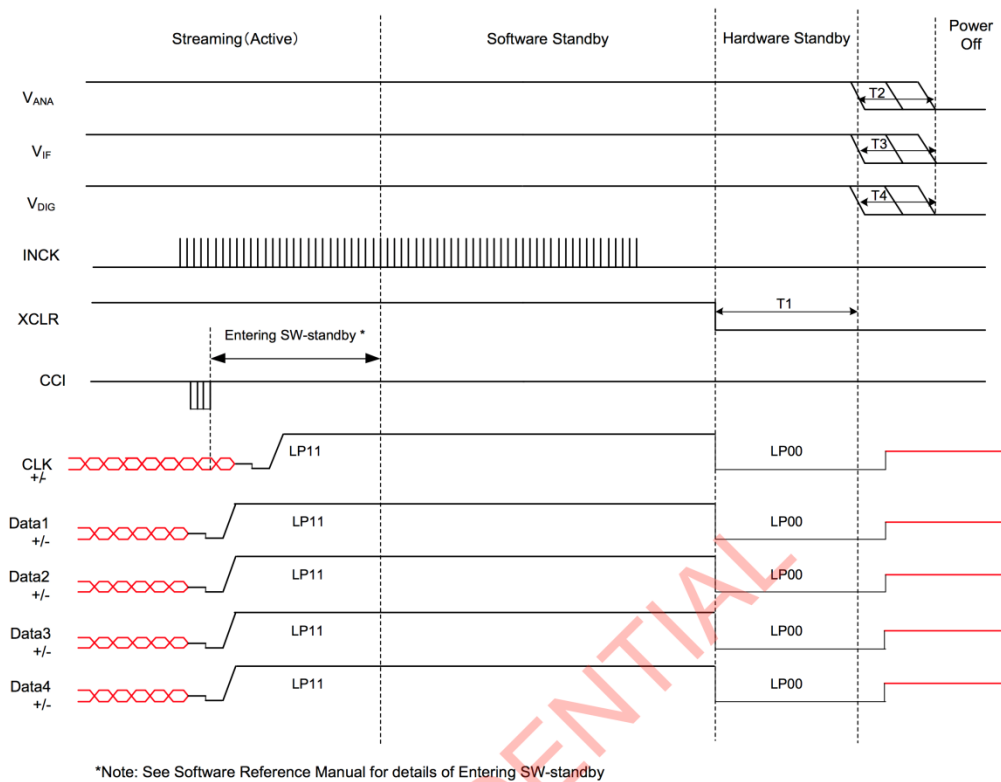
Note) XCLR needs to be Low until all power supplies complete power-on



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Power-off Sequence



Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge - V _{ANA} (V _{IF} or V _{DIG}) fall	T1	0		μs	Presence of INCK during Power Off is acceptable.
Sequence free of V _{ANA} falling and V _{IF} falling and V _{DIG} falling	T2,T3,T4	V _{ANA} and V _{IF} and V _{DIG} may fall in any order.		μs	



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Revision History

Revision	Description	Release Date
1.0	First Release	10. Feb. 2020



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